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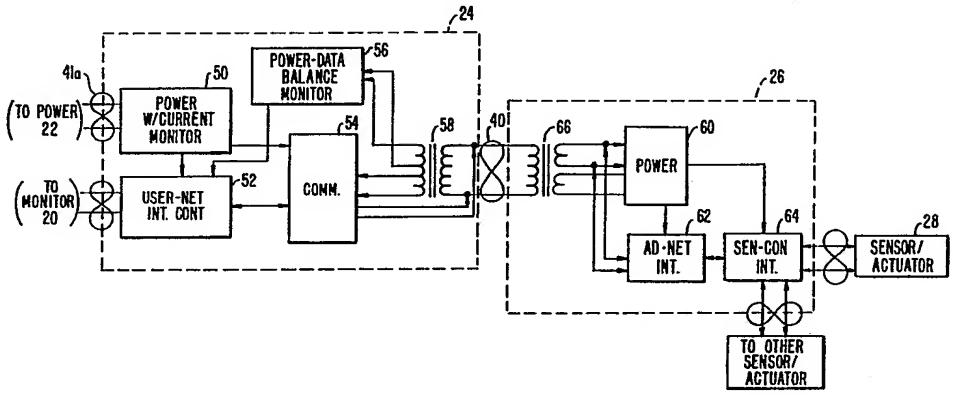

(57) Abstract

A computer network (10) using half-duplex communication to transmit digital data, including commands, addresses and responses, and power over a single MCI NETCON communication line (40). The network provides isolation to prevent a malfunctioning network device (28) from adversely affecting the system. Each device connected to the network includes an isolation transformer (58) to decouple devices with short circuit occurrences from properly functioning devices, permitting the network to continue to operate. A power-data balancing mechanism (56) reduces net dc-imbalances from the system, allowing cool and reliable operation of the transformers. Additionally, use a dynamic snubber (114) coupled to a power-data transmitter reduces inductive ringing in the network, improving power-data throughput.

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MONITORING AND CONTROL APPARATUS AND METHOD

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BACKGROUND OF THE INVENTION

The present invention relates generally to computer networks and more specifically to a network having one or more sensors or actuators (network devices) digitally communicated to and powered over a single conductive media, for example twisted pair cable, coaxial cable, or telephone wire.

Monitoring and control networks of the prior art have included a plurality of sensors powered and polled through use of a single pair of conductive media. These prior art networks typically time-multiplex simple control and power signals or use analog frequency-shift keying to control sensors of the network.

One example of an existing sensor operates at twelve to twenty four volts DC and provides information by a current loop. The prior art employed these sensors through use of a dedicated pair of wires per sensor.

Employing prior art monitoring and control networks using a single pair of conductive media for extensive network control applications can cause problems when one sensor malfunctions. A shorted sensor can disable the entire network, preventing the network's operation. For critical applications, it is unsatisfactory that failure of a single device could disable an entire network.

Another disadvantage of networks which time-multiplex data and power together is that data throughput speed is less than data throughput achievable if data transmission were

continuous. For systems which employ error detection or correction mechanisms which send redundant data, time-multiplexing degrades network speed even more.

SUMMARY OF THE INVENTION

The present invention provides method and apparatus for powering, controlling and monitoring a plurality of network devices over a single conductive medium, e.g. one twisted pair cable or coaxial cable, efficiently and safely. The invention achieves network device isolation through use of isolation transformers. The transformers prevent malfunctioning network devices from disabling other network devices commonly connected on the single conductive medium.

According to one aspect of the present invention, it includes a monitor, a power source, a network controller (NETCON) connected to the monitor and power source, and a network device. A network device adapter interfaces the network device to the NETCON. There may be multiple network devices per adapter, multiple adapters per network controller and multiple network controllers per monitor and power source. Each NETCON controls a subnetwork of each network device adapter and sensor or actuator coupled to it. Thus, one network may include a plurality of subnetworks, each controlled by one NETCON.

Multiple NETCONs effectively operate an overlapping set of network device adapters. Overlapping sets of network device adapters include network device adapters connected to two or more NETCONs by one or more conductive media. If a single conductive medium connects one NETCON to the adapters in one topological order, then connecting another NETCON to the adapters in a different topological order allows the network to operate and communicate with all the adapters and sensors/actuators if the conductive medium fails. As the number of NETCONs connected to the various adapters in various topological orders increases, the network's ability to control any particular adapter in the event of a fault improves. The network of the preferred embodiment employs a carrier sense, collision detection - multiple access (CSCD/MA) protocol to facilitate communications between the NETCONs and the adapters. Another solution to network operation

degradation provides multiple conductive media between a NETCON and the adapters.

The network controller and the adapters communicate with each other through the single conductive medium. The single conductive medium provides both (1) power for control, and (2) monitoring and powering of the adapters and network devices connected to the network controller. Transformers on the single conductive medium connecting the NETCON to the network device adapters, that is, at an adapter port and a network controller port, provide isolation for the network. The network controller includes a power-data balance mechanism which monitors signals over the conductive medium between the network controller and the adapters to ensure that the transmissions are substantially dc-balanced. The NETCON, and optionally each adapter, in one embodiment, includes a look-up table which provides a dc-balancing byte for each transmitted byte. The NETCON, and adapter, on a byte-by-byte basis, appends the dc-balancing byte to each transmitted character. Other embodiments could include real-time sampling of transmitted data to determine a net dc-imbalance, or net bit imbalance. Subsequent transmissions of balancing bits responsive to the sampled information produces balanced transmissions.

Another aspect of the invention provides a novel network controller including a communication circuit that shapes and processes digital data communicated over the medium between each NETCON and each adapter of its subnetwork. The communicated data has a particular amplitude and pulse-width characteristic, enabling the network controller to control, address, monitor and power its network devices and adapters without separate power and control lines. The term "power-data" refers to data having this particular characteristic.

To prevent degradation of the communication circuit or the isolation transformer resulting from a transmitted net dc-imbalance power-data packet, the novel network controller of one preferred embodiment includes a power-data balance monitor. The power-data balance monitor includes an power-data balance circuit to sense dc-imbalances in the network adapters' isolation transformers and to adjust the DC contributions of any appended

balancing bytes. Adjusting the balancing bytes reduces net dc-imbalances arising from operation of the network.

A substantially dc-balanced power-data packet allows use of smaller, cost effective isolation transformers which do not dissipate unnecessary heat. The cool operation of the transformer provides a more reliable system. The isolation of the network controllers from the network devices ensures a robust network which is not completely disabled by a single inoperative sensor or actuator. Provision of power and digital data combined in a single, two-way, half-duplexed signal in which a single medium carries high speed communication therefore contributes to a simple, cost effective installation and setup for the network.

One advantage of the present invention results from its ability to multiplex a plurality of current loop sensors on a single conductive media, rather than supplying each sensor with its own dedicated lines. A current loop interface in each network device adapter and the power-data signalling format permit implementation of this feature. The adapter employs an analog to digital converter, in one embodiment, to assist in the current loop interfacing to the NETCON.

The network is also able to employ effective error detection and correction circuitry for applications with critical data. In one preferred embodiment, both error detection and dc-balancing result from transmitting each critical power-data packet normally. The transmission is followed by a subsequent transmission of an inverted power-data packet having each bit of each power-data byte inverted.

Reference to the remaining portions of the specification and the drawing may realize a further understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a block diagram of a network 10 according to a preferred embodiment of the present invention;

Fig. 2 is a detailed block diagram illustrating the NETCON 24 and the MCI 26;

Fig. 3 is a timing diagram illustrating alternating cycles of power-data digital transmission and data receive;

Fig. 4 is a timing diagram illustrating an appendage of a set of balancing bits to a byte of a power-data packet;

Fig. 5 is a timing diagram illustrating an alternative power-data format for an alternate preferred embodiment of the present invention used with error detection;

Fig. 6 is a detailed block diagram of the NETCON 24;

Fig. 7 is a detailed block diagram of the power-data balance monitor 56 coupled to the isolation transformer 58;

Fig. 8 is a detailed diagram of the power-data transmitter 112;

Fig. 9A is a functional diagram illustrating the dynamic snubber 114;

Fig. 9B is a functional diagram illustrating an alternative dynamic snubber 114';

Fig. 10 is a flow chart illustrating a set of steps for the microcontroller 100 to execute which includes provision of dc-balancing of the isolation transformers 66 of the MCIs 26;

Fig. 11 is a detailed block diagram of the MCI 26 of Fig. 1 of one preferred embodiment;

Fig. 12A through Fig. 12C are flow diagrams for the preferred embodiments of programs executed by the microcontrollers used in the preferred embodiment of the present invention;

Fig. 12A is a flow chart illustrating the operation of the microcontroller 80 in the NETCON 24;

Fig. 12B is a flow chart illustrating the operation of the microcontroller 100 in the NETCON 24;

Fig. 12C is a flow chart illustrating the operation of the microcontroller 412 in the MCI 26; and

Fig. 13 is a timing diagram illustrating a biphase signal compared to a non-return to zero (NRZ) signal of the type employed in one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Table of Contents

I. General:

Fig. 1 is a block diagram of a network 10 according to a preferred embodiment of the present invention. The network 10 includes a monitor 20, a power source 22, a network controller (NETCON) 24, a network device adapter, referred to below as a monitor control interface (MCI) 26 and a network device, referred to as a sensor/actuator 28. The monitor 20 is a computer or an input/output device, for example, which provides selected network observation functions. Depending upon particular applications, the monitor 20 simply provides an information formatting function for the network 10 status. The individual NETCONs 24 provide the monitor 20 with status information for each particular sub-network the NETCON 24 controls. For other applications, the monitor 20 employs this status information and initiates various control and supervisory functions in the network 10 depending upon selected sensor/actuator 28 information. The monitor 20, in a preferred embodiment, is an appropriately programmed IBM PC-compatible personal computer (available from International Business Machines, Corp. of Armonk, N.Y.) running under MS-DOS (available from Microsoft, Corp. of Redmond, WA).

Each NETCON 24 of a preferred embodiment of the present invention controls operation of the MCIs 26 and sensors/actuators 28 of its subnetwork. Each NETCON 24 includes programmable processing functions to supervise subnetwork operations, including interfacing to the monitor 20 and providing addressing, command and power functions to the MCIs 26 and sensors/actuators

28, as well as receiving status information data from the MCIs 26. The MCIs 26 connected to each NETCON 24 all depend from a single conductive media 40 to form a multi-drop network as well known. In the preferred embodiment, this media 40 is a twisted pair cable and will be referred to below as an MCI communication line 40. To provide independent control and monitoring functions, each MCI 26 has an address. Each MCI 26 responds to commands directed to its address. The NETCON 24 provides power to the individual MCIs 26, and the sensors/actuators 28, over the same MCI communication line 40 which carries the addressing, command and status information data. In the preferred embodiment, every NETCON 24 transmission to the network powers each MCI 26 on the network, whether any particular MCI 26 is addressed or not.

Each MCI 26, powered by the NETCON 24 transmissions over the MCI communication line 40, interfaces and powers from one to many sensors in response to NETCON 24 commands. These commands initiate a sampling of particular sensors 28, or an operation of particular actuators 28. The NETCON 24, through the MCI 26, provides all power for the sensors 28, including actuators. Each NETCON 24 provides its data to and receives information from its monitor 20 and other NETCONs 24 through a user port using a RS-485 communication protocol. If the monitor 20 is sufficiently proximate a single NETCON 24, the user port may optionally include a converter to change the RS-485 signals directly to an RS-232 communication protocol. The RS-232 protocol is generally compatible directly with many personal computers. The RS-232 specification is hereby expressly incorporated by reference for all purposes.

In operation, the network 10 will include a plurality of NETCONs 24, a plurality of MCIs 26 for each NETCON 24, and a plurality of sensor/actuators 28 for each MCI 26. Each MCI 26 connected to a particular NETCON 24 will have both a "talker" address and a "listener" address. While only one MCI 26 is a talker for any particular address, one or more MCIs 26 can listen to a particular address. Talkers provide information to the network in response to particular commands from the NETCON 24 designated with their particular address. Listeners respond to

information prefaced with their particular address. NETCONs 24 and talker MCIs 26 provide listener MCIs with their information.

In one instance, the sensor/actuators 28 can include a thermocouple for temperature monitoring and an actuator to control operation of a cooling fan, for example. Each sensor/actuator 28 may be connected to a common MCI 26, or to two distinct MCI's 26. The NETCON 24 executes a prespecified program to control the cooling fan in response to the thermocouple information. Periodically, the NETCON 24 will poll, by addressing the particular MCI 26 connected to it, the thermocouple to measure a particular temperature. The particular MCI 26 samples an appropriate port connected to the thermocouple and returns temperature information to the NETCON 24. Another MCI 26 that controls the cooling fan will respond to a command to start the fan if the temperature information indicates a temperature above a prespecified level.

While the NETCON 24 controls this operation, in one embodiment it has many other sensors 28 to monitor and many actuators 28 to control. The information over the network 10 conforms to a desired protocol to ensure that the network 10 implements its necessary functions. The NETCON 24 provides all the power and data controlling this implementation over the single MCI communication line 40.

The monitor 20, in one embodiment, acts as a display for the network 10 status. The NETCONs 24, in the preferred embodiment, do not have displays or indicators providing status of each subnetwork comprised of each NETCON 24 and its sensors/actuators 28 and their MCIs 26. Therefore, each NETCON 24 periodically provides the monitor 20 with information regarding sensor/actuator 28 condition and general subnetwork status. The NETCON 24 of the preferred embodiment provides this information in ASCII format for easy display of the network 10 status. In another embodiment, the monitor 20 supervises operation of the network 10 and initiates particular predetermined operations depending upon various ones of the network 10 parameters which the NETCONs 24 communicate to the monitor 20. The monitor 20, in this embodiment, executes a program initiating events not otherwise preprogrammed into the

various NETCONs 24. This allows, among other things, coordination of actions among the various NETCON 24 controlled subnetworks.

Fig. 2 is a detailed block diagram illustrating the NETCON 24 and the MCI 26. The NETCON 24 includes power circuitry 50 having current monitoring features, a user-network interface controller 52, a communication circuit 54, a power-data balance monitor 56 and an isolation transformer 58. The MCI 26 includes a power circuit 60, an adapter-network interface controller 62, a sensor-controller interface 64 and an isolation transformer 66.

The power-data monitor 56, coupled to the MCI communication line 40 between a NETCON 24 and each MCI 26, generates signals indicative of a net dc-imbalance from data transmitted in a power-data packet, either a net positive dc-imbalance or a net negative dc-imbalance. These data packets pass through the isolating transformers 58 of the NETCON 24 and the MCI 26s' transformers 66. Knowing a relationship between parameters of the MCIs' transformers and the NETCON's transformer allows approximation of the net dc-imbalance effects upon the MCI 26s' transformers 66 at the NETCON 24. In one preferred embodiment in which the transformer 58 in the NETCON 24 is virtually functionally identical to the MCI 26s' transformers 66, then measuring net dc-imbalances of NETCON 24 transmissions through the NETCON 24's transformer effectively duplicates the effects of the power-data transmissions in the MCIs 26.

A controller of the NETCON 24 uses these signals to cause the communication circuit 54 to adjust the additional balancing bits appended to the transmitted power-data packet to cause the total transmitted data to substantially balance in a direct current sense.

The power circuitry 50 receives alternating current from the power source 22 over a user-NETCON cable 41a. The current monitor feature asserts a signal, OVR_I, if the communication circuit 54 draws excessive current. The user-network interface controller 52 provides the ASCII status information to the monitor 20 and can receive commands from the monitor 20 to initiate particular action with respect to a particular sensor/actuator 28. The user-network interface

controller 52 and the power circuitry 50 interface with the communication circuit 54 to control power and data relative to the network connected on the MCI communication line 40.

The user-network interface controller 52 includes a look-up table (not shown) which provides a balancing byte for each transmitted byte of a power-data packet. The user-network controller 52 compares each power-data byte the NETCON 24 will transmit to its table and appends 0 to n number of bits of balancing data to the byte, where n is a number of bits in each power-data byte. In other words, when each byte consists of a start bit, eight data bits and a command bit, for a total of ten bits, the NETCON 24 requires anywhere from 0 to 10 balancing bits to balance any particular byte. In a worst case situation, all bits have the same sense, requiring ten bits of opposite sense to balance. In the best case, five bits of one byte will have one sense and the other five bits of the byte will have an opposite sense. This five-five distribution requires no balancing bits.

The communication circuit 54, responsive to control signals from the user-network interface controller 52, transmits power-data to the subnetwork connected to the NETCON 24 over the MCI communication line 40. The communication circuit 54 includes transmitting functions and receiving functions. The isolation transformer 58 reduces the effect that a short circuit has on the entire subnetwork connected to the MCI communication line 40.

Transformer design in the prior art is well known, including trade-offs of size, efficiency and cost. The transformer 58 and transformers 66 are identical in one preferred embodiment. The isolation transformers include a plurality of windings, although in some instances the isolation transformer uses only two windings. For example, if the power-data balance monitor 56 were not implemented, the NETCON 24 would use two windings instead of the three shown. In one preferred embodiment that dispenses with the power-data balance monitor 56, the NETCON 24 uses optoisolators for isolation rather than the isolation transformer 58.

The transformers of a preferred embodiment are designed for 10 kHz conversion to supply nine volts and thirty volts from an input signal. The transformer efficiently provides two watts

through the thirty volt secondary and three watts through the nine volt secondary. The transformer has about 308 winds of about 34 gauge copper wire for one winding, about 315 winds of about 36 gauge copper wire on the thirty volt winding and about 132 winds of about 37 gauge copper wire on the nine volt winding. The transformer includes a size 1811 core made of 3C8 material. The nine volt supply will reduce to five volts while the thirty volt secondary supplies necessary voltage levels, that is twenty four volts rms, for current loop interfacing.

The communication circuit 54 implements some functions by coupling to a winding of the isolation transformer 58 and other functions directly to the subnetwork by bypassing the isolation transformer 58, as further defined below. For those functions implemented directly to the subnetwork on the MCI communication line 40, a preferred embodiment of the present invention uses optoisolators in the communication circuit 54 to prevent voltage spikes on the MCI communication line 40 from coupling to digital components, a digital ground or to the case.

The MCIs 26 receive power directly from the MCI communication line 40, the same line over which the subnetwork coupled to a NETCON 24 transmits digital data. The power circuit 60 includes regulator circuits which use relatively large capacitors for filtering and energy storage. In a preferred embodiment of the present invention, the power circuit 60 of each MCI 26 employs two 470 microfarad capacitors to permit operation when power is not present on the MCI communication line 40. A first regulator of the power circuit 60 supplies plus twenty four volts to power a current loop transmitter (not shown) of the adapter-network interface 62. A second regulator provides about 6.2 volts to power a modified RS-485 driver circuit of the adapter-network interface. The 6.2 volt regulator also, through appropriate scaling, provides about 5.0 volts for digital components of the MCI 26.

The adapter-network interface 62 includes transmitting and receiving functions (transceiver) supervised by a microcontroller (not shown). The microcontroller includes supporting circuits to provide memory, interrupts and clocking. The adapter-network interface 62 controls and supervises the

sensor/actuator 28 specific sensor-controller interface 64. For different implementations, a particular sensor or actuator 28 will require different interfacing circuitry to successfully connect and communicate to the adapter-network interface 62.

In operation, the MCI 26 receives commands and power over the MCI communication line 40. The preferred embodiment of the present invention implements an RS-485 specification for receiving and transmitting functions, except as noted herein. The RS-485 specification is hereby expressly incorporated by reference for all purposes. The adapter-network interface 62 receives, decodes and initiates actions dependent upon the received commands. The command can, for example, request a poll of a particular status of a particular sensor 28. The adapter-network interface 62 will obtain the necessary information by proper interface to the proper sensor 28 through the sensor-controller interface 64. After obtaining the information, the adapter-network interface 62 transmits the information to the requesting NETCON 24.

While for many applications, the RS-485 standard transceiving functions are adequate, the preferred embodiment of the present invention employs a modified RS-485 transceiver. The modifications to the RS-485 standard include: the ability to transmit power; decreased load, by a factor of 10, of receivers on twisted pair, and NETCON transmission at twenty four volts rms. These changes to the standard permit operation of 256 devices per NETCON 24 rather than the 32 of the standard.

Fig. 3 through Fig. 5 illustrate data formats for embodiments of the present invention. Specifically, Fig. 3 is a timing diagram illustrating alternating cycles of power-data transmission from the NETCON 24 and data transmissions from the MCIs 26. As illustrated, the communication circuit 54 of the NETCON 24, during the power-data transmit cycle, provides digital power-data which is +/- thirty volts for sixty volts peak-to-peak (which corresponds to +/- twenty four volts rms). The received data from an addressed MCI 26 is +/- six volts for twelve volts peak-to-peak.

One concern with power-data having this format, for example, when used with isolation transformers, is that any

particular transmitted packet may have a net dc-imbalance. As previously noted, the NETCON 24 is able to append a balancing byte to each transmitted power-data character byte through use of a look-up table. In one preferred embodiment, each MCI 26 transmits digital data to the NETCON 24. The digital data has an amplitude of about five volts rms. Thus, dc-imbalances arising from MCI 26 transmission is considered negligible, especially when power-data balance monitor 56 is used. It may be desirable, however, to have each MCI 26 implement a balancing mechanism for its transmissions. This mechanism is similar to the NETCON 24 mechanism. That is, the MCI 26 may either append balancing bits or invert each byte. By use of this system, substantial balancing of the energy through the subnetwork isolation transformers results.

The net dc-imbalance results from transmitted data which, when a total number of positive bits in the packet is compared to a total number of negative bits in the packet, does not have the total number of positive bits matching the total number of negative bits. A positive net dc-imbalance results from transmission of a greater number of positive bits than negative bits while a negative net dc-imbalance results from transmission of a greater number of negative bits than positive bits. The isolation transformers dissipate any net dc-imbalance as heat. Depending upon a severity of the dc-imbalance, dissipating the additional net dc-imbalance as heat degrades the transformer's performance. Excess heat can, for example, cause a ferrite core of the transformer to expand and perhaps crack. To provide maximum balancing through use of the look-up table, the MCI 26 responds to commands from the NETCON 24 to balance data it transmits. A preferred embodiment dispenses with balancing by the MCIs 26 to improve speed performance.

Fig. 4 is a timing diagram illustrating an appendage of a set of balancing bits to a power-data packet. For a power-data transmit cycle including from 1-512 power-data bytes, appending an appropriate polarity signal for 0-10 bit times will permit balancing of net dc-imbalance.

Fig. 5 is a timing diagram illustrating an alternative power-data format for an alternate preferred embodiment of the

present invention. In this alternate preferred embodiment of the present invention, dc-balancing is inherent in the structure of the power-data transmission format. This alternative preferred embodiment does not require a power-data balance monitor as each data packet which a NETCON 24 transmits is followed by an equivalent data packet with all the bit polarities inverted. Transmission of the inverted data packet immediately following the non-inverted packet exactly ensures that a net dc-imbalance does not develop from the NETCON 24 transmission. Other network conditions may cause a net dc-imbalance to develop, so a balance monitor 56 may be desirable. This alternate preferred embodiment also permits implementation of a straightforward error detection algorithm, as is known in the art. An incorrect comparison of the two power-data packets, the non-inverted and the inverted packet, results in the NETCON 24 of Fig. 2 retransmitting the data packet. This error detection and correction mechanism provides a network system with increased reliability. In one preferred embodiment of the present invention, each NETCON 24 is able to selectively function in either mode, error detection/correction or appended balancing bits, depending upon a criticality of any particular power-data packet.

The look-up table method of dc-balancing provides an approximation to the system to reduce excessive heat dissipation in the isolation transformer. The values of the balancing bytes, predetermined prior to operation, may not balance the network transmissions precisely enough for all applications over all operating ranges. Approximation of the balancing values alone can yield a net dc-imbalance through continual operation of the system. Rather than provide an unwieldy look-up table with many different values for different operating conditions and also to account for unanticipated net dc-imbalance conditions, one preferred embodiment couples the power-data balance monitor 56 through the isolation transformer 58 to the MCI communication line 40. As the isolation transformer 58 is identical to the isolation transformers used in each of the MCIs 26, in this configuration the power-data balance monitor 56 accurately measures, through integration and summing, the actual dc-imbalance of the network. Coupling the power-data balance

monitor 56 through the isolation transformer 58 allows measurement of any net dc-imbalances effects in the isolation transformers 66 of the MCIs by simulating those effects through the isolation transformer 58.

In a reliable, small and cost effective system which includes the transformer, the power-data balance monitor 56 of Fig. 2 has substantially eliminated actual net dc-imbalances resulting from operation of each subnetwork controlled by each NETCON 24. The power-data balance monitor 56, coupled to the output of the communication circuit 54, determines whether a the NETCON 24 transmitted a net positive or a net negative dc-imbalance. A determination that a net dc-imbalance exists causes the user-network interface controller 52 to adjust the table look-up values to alter the actual additional balancing bits appended to each byte of the transmitted packet to reduce the actual net dc-imbalance.

Fig. 13 is a timing diagram illustrating a biphase signal compared to a non-return to zero (NRZ) signal of the type employed in one embodiment of the present invention. Biphase encoding, also commonly referred to as Manchester encoding, is common in ethernet network systems. Biphase signals embed a clock signal in transmitted data, typically by "exclusive-OR"ing the data with the clock. The result produces an output waveform as shown in Fig. 13. Transmitting manchester encoded data does not result in inherent dc-balanced transmissions. A system employing Manchester encoding could none-the-less selectively modify the transmissions to produce dc-balanced transmissions. As shown, encoded "0" bits produce inherently dc-balanced data. Also, an even number of encoded "1" bits produce inherently dc-balanced data. Transmission of an odd number of encoded "1" bits imbalances a transmission. Thus, the present invention could monitor for an odd number of encoded "1" transmissions and provide a balance bit time of opposite dc sense to balance the net dc-imbalance contribution. The actual implementation of the balance bit time depends upon a block size and idle mode of the network. For one byte blocks, with steady state idle mode, one extra bit time of appropriate polarity appended to an output drive signal completes dc-balancing of the preceding

transmission.

Clock signal ouputs during idle mode provides continuous power with use of the isolation transformer. Bit times following the clock signal transmission balances the medium and the MCIs 26 ignore the extra bits. A clock consisting of all "0" bits or an even number of "1" bits is balanced. A change of the clock data bit indicates that a next data transmission is about to occur. For multi-master architectures, power clock cycle can be periodically interrupted for data block transmission.

Addition of a small signal load to the medium reduces noise. After the power cycle and prior to bias addition, the dynamic snubber 114 can improve data throughput as described herein.

II. Network Controller:

Fig. 6 is a detailed block diagram of the NETCON 24. Power circuitry 50 includes a digital power supply 70 and a power-data driver supply 72. The power source 50 also includes two power transformers 74 and 76 which interface the digital power supply 70 and the power-data driver supply 72, respectively, to the power source 22. The digital power supply supplies the voltages, for example +/- five volts, to the digital components of the NETCON 24. The power-data driver supply 72 provides the voltage levels for the power-data transmission, for example +/- thirty volts, to the communication circuit 54. The power source 50 incorporates a current monitor 78 to detect short circuits in the subnetwork. The current monitor 78, coupled to the power-data driver circuit 72, can monitor for an over current condition by detecting excessive current drawn from the power-data driver 72 by a transmitter of the communication circuit 54. If the current monitor 78 detects an over current condition, it asserts a signal which deactivates power-data transmitter 112 of the communication circuit 54.

Many different current monitoring circuits are available in the art. One preferred embodiment for a current monitor is to use a Hall effect device mounted in a gap of a

toroid through which a current in question flows. Integration of the output of the Hall effect device averages the current. A pulse width modulated technique filters the averaged current to provide current to voltage translation. Converting the current to a voltage permits an operational amplifier to generate the over current signal to the communication circuit 54 when the voltage exceeds a predefined reference value. Additionally, the current monitor 78 provides the voltage level to the user-network interface controller 52 for use in managing various network parameters.

The user-network interface controller 52 includes a user microcontroller 80 communicating to the monitor 20 by use of a data receiver 82 and a data transmitter 84. A user interface isolation transformer 86 isolates the NETCON 24 from the monitor 20. The data receiver 82 uses a high speed open-collector output comparator to sense a differential voltage at its inputs. A resistor and a capacitor, for example, filter the data receiver inputs. The data receiver is responsive to a transmit invert (TX_INVERT) signal from the user microcontroller 80 to invert a polarity sense of the input differential lines if a polarity reversal exists.

The data transmitter 84 provides signalling circuitry to output a differential square wave pulse train at baud rates up to 78,000 bits per second. The data transmitter 84 is responsive to three signals from the user microcontroller 80: a transmit enable signal (TX_ENABLE), a data signal (TX), and the TX_INVERT signal. TX is the data the data transmitter 84 is to transmit. The TX_ENABLE signal allows transmission of the data. The data transmitter 84 responds to an assertion of the TX_INVERT signal to invert a polarity sense for transmitted power-data to account for any miswiring in wiring connecting the NETCON 24 to the monitor 20, whether it is RS-232 or RS-485. The data transmitter 84 supports three logic states which are dependent upon a condition of TX_ENABLE and TX. Logic state one results when TX_ENABLE is off, placing all output transistors off. This is a tristate condition for the data transmitter 84. Logic state two results from asserting both TX_ENABLE and TX to pull one line of a differential output high and the other line of the differential

output to ground. In logic state three, with TX_ENABLE asserted and TX deasserted, the output line which was high has a transistor pulling it to ground while the previously grounded output line is now pulled high.

A ROM 90, a RAM 92 and a decode logic 94 implement a standard mechanism, as well known in the art, for mapping memory and logic to a microcontroller such as an 80C51. The ROM 90 stores the computer code which the user microcontroller 80 executes to perform its various predefined functions, which include control of the transmit and receive functions of the data transmitter 84 and the data receiver 82.

The user-network interface controller 52 includes a second microcontroller, a network microcontroller 100. The network microcontroller 100 functions to monitor the NETCON 24 functions and control the NETCON's activities relative to the subnetwork coupled to the MCI communication line 40. A second ROM 102, a second RAM 104 and a second decode logic 106 implement a standard memory and logic mapping mechanism, similar to that of the ROM 90, RAM 92 and the decode logic 94.

The two microcontrollers, the user microcontroller 80 and the network microcontroller 100 share a common dual port RAM 110. The dual port RAM 110 permits communication between a user side of a subnetwork, the monitor 20, and the subnetwork itself. Both microcontrollers control the dual port RAM 110 through standard mechanisms as well known in the art. A busy signal prevents a semaphore condition in the user-network interface controller.

The communications circuit 54 includes a data receiver 110, a power-data transmitter 112 and a dynamic snubber 114. The data receiver 110, in the preferred embodiment, is identical to the data receiver 82.

The power-data transmitter 112 is similar to the data transmitter 84 functionality. The power-data transmitter 112 includes an additional function of supplying digital data with an amplitude and pulse width characteristic which permits the NETCON 24 to deliver subnetwork operating power in a digital bit stream. The output waveform, in a preferred embodiment, is a square wave pulse train having an amplitude of +/- thirty volts (for twenty

four volts rms) and a variable pulse width of about one to ten serial bit times, which is about 48 to 480 microseconds in one preferred embodiment. This characteristic is alterable depending upon subnetwork power requirements and parameters of the isolation transformers and the power supplies/power regulators of the MCIs 26. The power-data transmitter 112 of a preferred embodiment consists of an inductor-capacitor ladder network. This inductor-capacitor ladder network is a low pass filter providing high frequency noise filtering. The power-data transmitter 112 includes power MOSFETs as current drivers and optoisolators for decoupling signals on the MCI communication line 40 from the digital power supply 70 and the power-data power supply 72.

The dynamic snubber 114, coupled directly to the subnetwork through direct connection to the MCI communication line 40, is a unique specialized circuit of the preferred embodiment to enhance network communication speed. When the microcontroller 100 turns off the power-data transmitter 112's drivers, the dynamic snubber 114 dissipates energy on the MCI communication line 40. Without the dynamic snubber 114, inductive ringing will start after transmission of the last bit from the power-data transmitter 112, causing extraneous data transmission while the communication line "settles." Unless a programming of each MCI 26 requires that the MCI 26 delay a predetermined time before communicating to ensure settling of the inductive ringing on the MCI communication line 40, the ringing can cause MCIs 26 to fail to respond or respond to an incorrect address. The delay solution degrades communication speed performance.

Functionally, the dynamic snubber 114 is a timed switch which dynamically loads the MCI communication line 40 after each power-data packet communication to damp any inductive ringing. The dynamic snubber 114 is responsive to the TX_ENABLE signal of the power-data transmitter 112 to control the loading of the MCI communication line 40. Termination of a transmission results from deassertion of the TX_ENABLE, which couples a load between the MCI communication line 40 leads and ground. Deassertion of the TX_ENABLE also begins a timer which will open the switch

after elapse of a prespecified time. In the preferred embodiment, the dynamic load is purely resistive, about 100 ohms, and remains coupled for about 40 microseconds. Variations to these values are possible depending upon performance and loading required to damp any inductive ringing. The load may require a complex impedance for optimal operation. Optoisolators, not shown, decouple the MCI communication line 40 from the digital power supply 70 and the power-data supply 72.

The optoisolators also provide a switching function. Proper selection of an acceptable optoisolator in any particular application should consider that optoisolators can have an output transistor saturation problem producing unequal turn-off and turn-on times. Significant inequality in the two times results in short circuits of the driver circuits for nanosecond periods, or greater. These short circuits cause the drivers to dissipate more power which increases cooling requirements of the NETCONs 24. Additionally, the output transistors of some optoisolators only have limited current capacity, with current capacity affecting switching speed. One example of an acceptable optoisolator for the preferred embodiment of the present invention described herein uses optoisolators such as the Siemens ILCT6, a gallium arsenide infrared light emitting diode (LED) with a silicon NPN phototransistor that has a 50% current transfer ratio, for example. The 50% current transfer ratio prevents the NPN phototransistor from saturating.

Fig. 7 is a detailed block diagram of the power-data balance monitor 56 coupled to the isolation transformer 58. The signals the power-data balance monitor 56 uses to establish an existence of a net dc-imbalance include the power-data and response data as shown in Fig. 4, for example. These signals have an amplitude of +/- thirty volts (+/- twenty four volts rms) in the preferred embodiment. Therefore, in sampling these signals, diodes D_1 and D_2 permit separation of the positive sense signals from the negative sense signals. Two integrators, a high integrator 200 for positive sense signals and a low integrator 202 for negative sense signals, sample the signals on the MCI communication line 40 through the isolation transformer 58. A summing amplifier 204 sums both of the integrated high and low

sense signals. The preferred embodiment of the present invention provides the summing amplifier 204 with an amplification value of about unity.

Two voltage comparators, a net high dc-imbalance comparator 210 and a net low dc-imbalance comparator 212 provide triggering for assertion of a NET_HIGH signal and a NET_LOW signal, respectively. A high-trigger voltage reference 214 sets a predetermined high trigger point for the net high comparator 210 as well known in the art. A low-trigger voltage reference 216 sets a predetermined low trigger point for the net low comparator 212 as well known in the art. For the preferred embodiment, the high and low voltage trigger points are about +/- one-tenth volts, respectively.

A complex impedance filter network 218 for the net high comparator 210 and the net low comparator 212 provide filtering for the outputs of the comparators to ensure a proper sampling period. For the preferred embodiment of the present invention, a minimum of two byte times of sampling occurs for the output signals. The net high comparator 210 asserts the NET_HIGH signal if the summation of the high integrator 200 output and the low integrator 202 exceeds the high trigger voltage. Similarly, the net low comparator 212 asserts the NET_LOW signal if the summation of the high integrator 200 output and the low integrator 202 exceeds the low trigger voltage.

The microcontroller 100, see Fig. 6, uses the NET_HIGH and the NET_LOW signals digitized by the analog to digital convertor to alter any balancing bit values it appends to each byte of a transmitted power-data packet. Assertion of NET_HIGH results in the microcontroller 100 decreasing the values of the balancing bits, that is appending fewer bits, while assertions of NET_LOW results in an increase (more bits) of the values of the balancing bits derived from the look-up table.

Fig. 8 is a detailed block diagram of the power-data transmitter 112. The power-data transmitter includes a control logic block 220, optoisolators 222, current drivers 224 and a low pass filter 226. The control logic block 220 responds to the input signals TX, TX_INVERT, TX_ENABLE, and OVR_I. The TX, TX_INVERT, and TX_ENABLE signals from the microcontroller 100

operate as described above. Assertion of TX_ENABLE drives the outputs according to the data presented on TX. Assertion of TX_INVERT indicates a polarity reversal in the system, so the signals are driven at the output of the power-data transmitter 112 in a polarity sense opposite that of the what it would be without the TX_INVERT asserted. Deassertion of TX_ENABLE tristates the output of the power-data transmitter 112 and activates the dynamic snubber 114 immediately upon the deassertion. Assertion of the OVR_I signal from the current monitor 78 disables the output of the power-data transmitter 112. Depending upon the status of the input signals, the control logic block 220 will selectively enable particular output transistors in each of the optoisolators 222, if an output is driven. These particular selected transistors of each optoisolator act as switches to control a particular voltage to appear at an output of the driver circuits 224. For example, assertion of TX and TX_ENABLE, without assertion of TX_INVERT or OVR_I signals, results in coupling a V^+ voltage of the power-data supply 72, in Fig. 6, to a NET_A line (one conductor of the MCI communication line 40, for example) and a coupling of a V^- voltage to a NET_B line (the other line of the MCI communication line). For a deassertion of the TX signal, the power-data transmitter 112 couples the V^- voltage level to the NET_A line and the V^+ voltage level to the NET_B line. The low pass filter 226, an inductor-capacitor ladder, removes high frequency noise.

Fig. 9A is a functional diagram illustrating the dynamic snubber 114. The dynamic snubber 114 includes an impedance 230 and a switch 232, controlled by a switch control circuit 234 responsive to the TX_ENABLE signal. In a preferred embodiment an optoisolator (not shown) decouples the switch control 234 from an output transistor which functions as the switch 232.

In operation, a deassertion of the TX_ENABLE signal initiates the switch control 234 to couple the NET_A and the NET_B lines of the MCI communication line 40 together by the switch 232. A bridge rectifier allows a mono direction switch (transistor) to be used for the switch 232. The switch control 234 includes a timer to open the switch after a predetermined

interval. In the preferred embodiment, a 555 timer limits the switch 232 closure duration to about 40 microseconds. An embodiment of the present invention employing the dynamic snubber 114 damps any inductive ringing occurring after cessation of transmission rapidly enough that the MCIs 26 are not required to wait to respond. This damping of the inductive ringing occurs fast enough that the subnetwork is virtually unaffected by the inductive ringing, allowing rapid two-way half-duplex communication over the MCI communication line 40.

Fig. 9B is a functional diagram illustrating an alternative dynamic snubber 114'. The dynamic snubber 114' includes an impedance 230 and a combined switch and a switch control circuit 234' responsive to the TX_ENABLE signal. In a preferred embodiment, the impedance 230 comprises existing power MOSFETs of the driver circuit 112.

In operation, a deassertion of the TX_ENABLE signal initiates the switch control 234' to couple the NET_A and the NET_B lines of the MCI communication line 40 together by the power MOSFETs of the driver circuit 112. The switch control 234' includes a timer to open the switch after a predetermined interval. In the preferred embodiment, a 555 timer limits the snubber 114' duration to about 40 microseconds. An embodiment of the present invention employing the dynamic snubber 114' damps any inductive ringing occurring after cessation of transmission rapidly enough that the MCIs 26 are not required to wait to respond. This damping of the inductive ringing occurs fast enough that the subnetwork is virtually unaffected by the inductive ringing, allowing rapid two-way half-duplex communication over the MCI communication line 40.

Fig. 10 is a flow chart illustrating a set of steps for the NETCON 24 to execute to provide dc-balancing of the isolation transformers 66 of the MCIs 26. Step 300 through step 324 depict a set of typical steps for transmission of data to an MCI 26. Initially, the microcontroller 100 determines whether it has any data for transmission (step 302). Assuming data for transmission exists, the microcontroller 100 reads a byte for transmission (step 304). A transmission packet in the preferred embodiment includes from 1 to 512 bytes, and the microcontroller 100 appends

a balancing byte to each data byte. The microcontroller 100, after reading a particular byte (step 304), uses the 10-bit byte value to access a look up table storing a correlation of precalculated balancing bits for each byte character (step 306).

After the microcontroller 100 accesses a value of the balancing bits (steps 306), it appends the balancing byte to the byte it is to transmit (step 308). The microcontroller 100 initiates transmission of the packet (step 310), including all bytes with appended balancing bits by proper assertion of the TX, TX_ENABLE and TX_INVERT signals.

After appending and transmitting balancing byte (steps 306, 308 and 310), the microcontroller 100 determines if the balancing bits require an adjustment (steps 312, 314, 316 and 318) based upon an averaging over at least two byte times of transmission. At step 312, the microcontroller 100 determines if the power-data balance monitor 56 is asserting the NET_HI signal. An assertion of the NET_HI signal indicates a positive net dc-imbalance in the isolation transformers of the MCIs 26 on the NETCON 24's subnetwork. Therefore, the microcontroller 100 decreases a magnitude of positive charge, as reflected in the value of the balancing bits, to decrease the positive net dc-imbalance (step 314). Similarly, if the power-data balance monitor 56 asserts NET_LO (step 316) and not NET_HI, the microcontroller 100 increases a magnitude of positive charge to decrease a negative net dc-imbalance (step 318).

Upon termination of the packet transmission (TX_ENABLE deasserted), the dynamic snubber 114 damps any inductive ringing (step 320). The microcontroller 100 waits for a response from an MCI 26 (step 322) after which the NETCON 24 returns to transmit more data, if necessary (step 302). If there is no data for transmission, the balancing procedure terminates (step 324). Note that if the microcontroller 100 does not have data for transmission, it will periodically transmit an idle pattern consisting of five-five in hexadecimal format. This data pattern allows the MCIs 26 to synchronize to the NETCON 24 data. The frequency of these refreshing cycles depends upon particular characteristics of the MCIs 26 and the power-data transmission values.

III. Monitor and Control Interface:

Fig. 11 is a detailed block diagram of the MCI 26 of Fig. 1 of one preferred embodiment. The power circuit 60 includes two regulator circuits, a twenty four volts rms regulator circuit 402 and a 6.2 volts rms regulator circuit 404. These regulator circuits include a diode bridge, a storage capacitor and a regulator. The regulators receive transformer-coupled power-data signals from a transmission on the MCI communication line 40, rectify, store and regulate the voltages from the transformer 66. As shown, applying the 6.2 volt output across a series of diodes provides a nominal five volts for digital power. The twenty four volts powers a current loop transmitter of the MCI 26. The 6.2 volts powers the modified RS485 transceiver 410.

The adapter-network interface 62 includes the modified RS-485 transceiver 410 coupled to a masked programmed microcontroller 412. One example for a preferred embodiment of the microcontroller is an 80C51 manufactured by Intel Corporation of Santa Clara, California. The masked programmed microcontroller 412 implements a simplified embodiment of the invention which only performs monitoring functions. The on-chip ROM is pre-programmed, in one preferred embodiment, to respond to six simple commands identified in a command table. These six commands are commands causing the MCI 26 to read a particular one channel. That is, command one reads channel one. The channels have predetermined functions such as channel one could correspond to a particular temperature sensor in a particular range. Channel two could correspond to measurement of a thermocouple having some other range. This configuration does not offer complete programming capability but is an order of magnitude less expensive than a fully programmable unit. The fully programmable unit of the preferred embodiment includes a general purpose microcontroller 412 having an internal non-volatile memory section. This non-volatile writable memory includes a configurable command table able to store 255 different commands. This system provides commands for control in addition to simple

monitoring functions. The MCI 26 is programmable to particularly respond to any one of 255 different commands.

In addition to the on-chip memory, the microcontroller 412 uses a nonvolatile RAM 414, a watchdog timer 416 and an LED addressing indicator 418. The nonvolatile RAM 414 stores configuration data for the MCI 26, such as addresses and calibration data. Also, the non-volatile memory stores location of sensors. The watchdog timer 416 prevents the masked programmed microcontroller 412 from executing out of sequence instructions. The LED addressing indicator 418 serves a diagnostic function to visually indicate when a network apparatus addresses the MCI 26. The microcontroller 412 communicates to the modified RS-485 transceiver 410 through four communication lines. These lines include an invert receive data enable signal, a receive data in signal, a transmit data out signal and a transmit enable out signal.

The sensor-controller interface 64 includes a sensor/actuator interface circuit 450 and a current loop transmitter interface circuit 452. The configuration of the sensor/actuator interface circuit 450 depends upon the type of network device 28 it operates. The interface circuit 450 includes, for example, a thermocouple interface, an RTD interface, a thermistor interface or a zero to five volt interface. The current loop transmitter interface circuit operates as known in the art to receive an indication from sensor-type network devices. The indication is an amount of sensor attenuation of a current the current loop transmitter provides representing the sensor reading.

The sensor-controller interface 64 also includes an eight to ten bit analog to digital converter 460, an analog to digital voltage reference circuit 462, an on-board ambient temperature sensor 464. The analog to digital converter 460 responds to signals from the microcontroller 412 to appropriately operate the network device interface 450. The analog to digital converter 460 converts, responsive to a reference voltage from the voltage reference circuit 462 and the temperature circuit 464, the current transmitter loop information to digital form for the microcontroller 412. The temperature sensor 464 provides on-

board compensation for any temperature drift of the sensor-controller interface 64. Additionally, the temperature sensor 464 provides temperature information to the microcontroller for transmission by the MCI 26 as an indication of temperature in the particular MCI 26 vicinity. The temperature sensor 464 in this mode provides temperature information to the network just as any temperature sensor 28 connected to the sensor-controller interface 64 would.

IV. Program Description:

Fig. 12A through Fig. 12C are flow diagrams for the preferred embodiments of programs executed by the microcontrollers 80, 100 and 412. The code executed by the microcontrollers, (source code included in the appendices attached hereto and incorporated by reference for all purposes) operate to implement the functions described herein. The included source code is written using an 8051 cross assembler, operated on an IBM-PC compatible machine.

Fig. 12A is a block diagram illustrating the operation of the microcontroller 80 in the NETCON 24. This microcontroller 80 oversees operation of the NETCON 24 and its associated MCIs 26 and sensors/actuators 28. As shown, step 500 initializes the network upon power-up or reset. The initialization starts a NETCON 26 command processor procedure as well as a scanning procedure for data in the dual-port memory. The initialization procedure stores a predetermined set of MCI commands in the dual port memory 110. The dual port memory 110 has a first block of memory reserved for MCI commands. In the preferred embodiment, each NETCON 24 controls a maximum of 255 MCIs 26. Each MCI 26 has eight channels, with six of them being read channels. The maximum reserved memory size of the first memory block of the dual port memory 110 is about two kilobytes (255 x 8). The initialization procedure loads commands for each channel of each MCI 26 with its appropriate start-up command. If the system does not use a particular channel of an MCI 26 or a particular MCI 26, then the microcontroller 80 loads a no operation indicator, zero for example, into that location.

The architecture of the preferred embodiment of the present invention provides a unique address in a second block of memory of the dual port RAM 110 for each MCI 26 attached to its NETCON 24. The microcontroller 80 polls these addresses for data from each particular MCI 26 in step 502. Upon finding data, the microcontroller 80 determines an appropriate response to the data. The polling of step 502 also includes monitoring a third block of memory of the dual port RAM 110 that records any limit errors, status errors or other exceptions detected by the NETCON 24. This polling continues to cycle through all the MCI 26 addresses. In this mode, the NETCON 24 controls the subnetwork operation according to the predetermined program.

One embodiment of the present invention has the microcontroller 80 also being responsive to command requests from a user such as the monitoring device 20 or another NETCON 24. Receipt of an interrupt operation, such as a command request from the user, can cause the microcontroller 80 to execute a different set of processes. Step 504 waits for a command request from the user. If a user command request occurs, the microcontroller executes step 506 to process the command. Processing of the command request may result in no change to the MCI command sequences in the first block of memory. The command request could seek information from a different MCI 26 or a different channel of an MCI 26 not previously monitored. In this case, the microcontroller 80 will overwrite the previous commands in the first memory block to acquire the necessary information. After obtaining the information, the microcontroller 80 can restore the commands or continue under the revised set of commands. Step 504 and step 506 continue to cycle and operate substantially concurrently with the step 502. These operations as described above result from execution of code compiled from the source code included in appendix A1.

Appendix A1 includes a number of modules. These modules form the NETCON network interface. The NETCON network modules include NNET-BIT, NNET-MAN, NNET-DP, NNET-PMG, NNET-IOP and NNET-NVR as well as a number of library files which include: NLIB-DCD, NLIB-MTH and NLIB-NVR.

NNET-BIT contains the NETCON User Interface bit definitions. The NNET-MAN is the main program loop of the NETCON User Interface. After a reset, operations begin here. This loop contains all the main program and interrupt entry points. The NNET-DP contains the dual port routines for the NETCON User Interface. These routines facilitate communication with MCI-communication processor identified as MNET. The NNET-PMG is the command processor of the NETCON User Interface. NNET-IOP is the network processor of the NETCON User Interface. This module receives and sends commands to other NETCONs or to the monitor/display personal computer. NNET-NVR include the NETCON's RAM routines. Serial number and other related documents are stored here.

The library module NLIB_OCD is a command input parser used to decode commands from both the user and/or other NETCONs. NLIB-MTH includes math routines and formatted input data routines. NLIB-NVR includes the nonvolatile RAM hardware interface routines.

Fig. 12B is a block diagram illustrating the operation of the microcontroller 100 in the NETCON 24. Step 530 through step 540 do the tactical work of sending dc-balanced power-data to each MCI 26, receiving data from the MCIs 26 and ensuring smooth operation of the subnetwork the NETCON 24 controls as efficiently as possible. Step 530 initializes the microcontroller 100 controlled elements, such as the dual-port memory, the MCI network serial interrupts, the MCI network timer interrupts and the MCI network balanced transmission type. Step 530 also begins a scan of the first memory block addresses to determine the commands to issue to the various MCIs 26. The microcontroller 100 causes the NETCON 24, at step 532, to issue its command as a request to a particularly addressed MCI 26. The request may include a plurality of bytes of data. After requesting the particularly addressed MCI 26, the microcontroller will wait about two character time delays for a reply from the MCI 26. If no reply occurs within the specified time, the microcontroller 100 returns to step 532 to access the next address to obtain a command for a next MCI 26. Each time the microcontroller 100 completes a full scan of all the MCI 26

addresses, the microcontroller 100 initiates transmission of a synchronization character. In the preferred embodiment, sending a five-five hexadecimal character enables MCIs 26 to check wiring polarity. If an MCI 26 does not receive what it recognizes as the synchronization character within a particular time, it causes the receiver to invert its inputs, inverting any signal received at the MCI 26 port. Periodically issuing the synchronization character allows dynamic addition of additional MCIs 26 without stopping and restarting a particular subnetwork. The microcontroller 100 dc-balances transmissions from the NETCON 24 as described above.

Terminating transmission of each power-data packet causes the microcontroller 100 to enable the dynamic snubber 114 at step 536. After receiving a reply, the microcontroller 100 saves the data at the appropriate location in the second block of memory and checks for limit errors in the data at step 538. If the microcontroller 100 detects no errors, it returns to step 532. Detecting an error, however, causes the microcontroller 100 to execute step 540 to load the error status into the third block of the dual port memory 110.

Appendix A2 includes a number of modules. These modules form the MCI network controller software and include code for transmitting dc-balanced power-data to the MCIs 26 and to scan all MCI 26 addresses for command requests and to place replies in appropriate locations of the dual port RAM 110. Execution of code compiled from source code including the appendix A2 listings execute the functions described above for the microcontroller 100.

MNET-BIT includes the Network controller bit definitions. MNET-MAN is the main program loop executed after reset. This loop contains all the main program and interrupt entry points. MNET-IOP is the balanced data power transmitter and receiver. It includes a data/command decoder which calls the NET-CMD file after a command is received. NET-CMD is the command action routines called from MNET-IOP to define actions executed for each command received. MCI-CMD includes the command tables for talk and listen addresses and setting command reply counts. MCI-BAL includes the balance table maintenance routines. These

tables contain the balance time required for each data byte. MNET-DP include the dual port memory routines which facilitate communication with the NETCON network processor (NNET).

Fig. 12C is a block diagram illustrating the operation of the microcontroller 412 in the MCI 26. Step 550 through step 562 are a set of processes for a preferred embodiment of the present invention. Step 550 initializes the MCI 26 and begins a command interpreter to determine particular operations to perform upon receipt of a valid command request. Before processing occurs, the preferred embodiment waits until an input character equals a synchronization character, or an inverted synchronization character. Upon detecting a synchronization character, the program execution advances to step 554 to wait for a synchronization frame. The synchronization frame consists of a string of 20 characters of data 55H. If the microcontroller 412 detects an inverted synchronization character, the microcontroller 412 causes the transceiver 410 to invert received data at step 556. If the received data does not match with the synchronization character, or its inverse, a delay is initiated prior to receiving the next character to supply a bit synchronization time. If the received data matches with the desired synchronization character, a counter is set to a minimum synchronization count and a next character is tested to match the synchronization character. If the data matches with the inverse of the synchronization character, the receive polarity is reversed, a counter is set to the minimum synchronization count and the next character is tested to match the synchronization character. If at any time during the synchronization character count down process a non-matching character is received, the process restarts. If the required number of synchronization characters are found, the MCI waits for the first command character to start processing the desired command.

After receipt of the synchronization frame, the microcontroller 412 waits for receipt of its command at step 558. The microcontroller 412 processes the command at step 560 to determine the functions it is to perform for the received command request. The microcontroller 412 refers to an internal command table to establish the appropriate activity for a received

command. At step 562, the microcontroller 562 reads input data from the sensor 28 attached to the channel identified by the command request. Alternatively, the command request could identify actuators 28 on one or more channels of the MCI 26 that the microcontroller 412 is to operate. For read data, the microcontroller 412 conditions the data, for example by converting current from a current loop transmitter to a voltage that the analog to digital converter 460 changes into digital levels. Additionally, the microcontroller 412 updates local control points which include, depending upon particular embodiments, various combinations of sixteen input and output ports. In the preferred embodiment, there can be a maximum of eight input ports and eight output ports operating simultaneously. Each port can be digital or analog. Digital ports can have up to eight data bits. The analog ports can have from eight to sixteen data bits, depending upon desired resolution. It is possible, on the MCI, to combine both digital ports and analog ports. Output ports are capable of driving standard actuator devices.

Appendix A3 includes nine modules. These modules include code for detecting and correcting polarity inversion of input data, command interpreter functions, sensor reading and conditioning, actuator operation and data transmission functions. Execution of code compiled from source code including the appendix A3 listings execute the functions described above for the microcontroller 412.

Module MI-BIT includes the MCI bit definitions. Module MI is the main MCI program loop. After reset, the operations begin here. This module includes all main program and interrupt entry points. Module MI-IOP is the MCI network command receiver and processor, including synchronization routines. Module COMMAND is the MCI command decode table. Module MCI-BAL are the command balance table maintenance routines. The tables include the balance time required for each data byte. Module MI-A2D are the MCI analog input routines. Input calibration and averaging and scaling the desired inputs to output quantities, e.g. 68°F, 100psia, 50%RH, etc. Module MI-NVR is the nonvolatile storage of serial number, scale factor, talk address, listen address, etc.

Module EEPROM includes the low level hardware interface to the nonvolatile RAM. Module MI-MATH includes the math routines used to scale the analog to digital readings and supply miscellaneous functions.

V. Conclusion:

In conclusion, the present invention offers advantages over prior art systems. The use of isolation transformers allows safe and efficient system operation of a network that supplies power and digital data through a single conductive medium. Transmitting balanced power-data facilitates use of the isolation transformers by reducing implementation and maintenance costs of the network. The dynamic snubber speeds network throughput by reducing delays introduced in response to inductive ringing.

While the above is a complete description of the preferred embodiments of the present invention, various alternatives, modifications and equivalents are possible. Therefore, the above description does not limit the scope of the present invention. The appended claims define the scope of the invention.

WHAT IS CLAIMED IS:

1. A network controller, comprising:

a power circuit;

a communications circuit, coupled to said power circuit, for transceiving data with respect to a port of the network controller; and

a user-network interface controller, coupled to said power circuit and to said communication circuit, for processing power-data for transmission to said port by said communication circuit, said user-network controller interface implementing a dc-balancing mechanism to substantially dc-balance transmissions of said communication circuit.

2. The network controller of claim 1 wherein said power-data for transmission includes at least one byte and wherein said dc-balancing mechanism includes a look-up table responsive to said at least one byte, said look-up table storing a particular predefined balancing character for said at least one byte which substantially dc-balances said at least one byte, said dc-balancing mechanism appending said predefined balancing character to said at least one byte for transmission.

3. The network controller of claim 1 wherein said power-data for transmission includes at least one byte including a plurality of bits and wherein said dc-balancing mechanism includes means for producing an inverted byte wherein said inverted byte has a plurality of bits with each bit of said inverted byte equivalent to an inversion of each bit of said plurality of bits of said at least one byte, said dc-balancing mechanism providing said inverted byte to said communication circuit so said communication circuit can transmit said at least one byte and said inverted byte.

4. The network controller of claim 1 wherein said power circuit comprises a first supply coupled to said communication circuit to provide power for said power-data and a second supply, and said network controller further comprises

means for isolating said first supply from said second supply.

5. The network controller of claim 4 wherein said isolating means comprises an isolation transformer, said isolation transformer including a first winding coupled to said communication circuit and a second winding coupled to said port.

6. The network controller of claim 1 further comprising an isolation transformer having a first winding coupled to said communication circuit and a second winding coupled to said port.

7. The network controller of claim 2 further comprising an isolation transformer having a first winding coupled to said communication circuit and a second winding coupled to said port.

8. The network controller of claim 1 wherein said power-data for transmission includes biphase data produced by an exclusive logical sum of a clock signal and data for transmission.

9. The network controller of claim 8 wherein said dc-balancing mechanism includes means for appending a balance bit to a transmitted biphase data packet having an odd number of binary high bits.

10. The network controller of claim 6 further comprising a power-data balance monitor coupled to a third winding of said isolation transformer and to said user-network interface controller, for detecting a net dc-imbalance at said third winding and asserting a signal to said user-network interface controller when it detects a dc-imbalance to influence said dc-balancing mechanism.

11. The network controller of claim 7 further comprising a power-data balance monitor coupled to a third winding of said isolation transformer and to said user-network

interface controller, for detecting a net dc-imbalance at said third winding and asserting a signal to said user-network interface controller when it detects a dc-imbalance to alter said predefined balancing byte appended to said at least one byte.

12. A monitor and control interface, comprising:

an isolation transformer;

a power circuit, coupled to a first winding of said isolation transformer, for receipt of a transformer-coupled power-data packet transmitted to a second winding of said isolation transformer to generate operating power from said transformer-coupled power-data packet for the monitor and control interface;

a sensor-controller interface, powered by said power circuit, for interfacing at least one network device which includes providing power to operate said at least one network device; and

an adapter-network interface coupled to said first winding and to said sensor-controller interface, said adapter-network interface powered by said power circuit and responsive to said transformer-coupled power-data packet to control operation of the monitor and control interface.

13. The monitor and control interface of claim 12 further comprising means, coupled to said adapter-network interface, for transmitting information.

14. The monitor and control interface of claim 12 further comprising a conductive medium coupled to said second winding wherein said adapter-network interface includes means, coupled to said first winding, for detecting an inverted coupling of said conductive medium to said second winding.

15. The monitor and control interface of claim 14 wherein said conductive medium comprises twisted pair cable.

16. The monitor and control interface of claim 14 wherein said adapter-network interface further includes means for

automatically correcting said detected inverted coupling of said conductive medium to said second winding.

17. The monitor and control interface of claim 12 wherein said isolation transformer comprises a ferrite pot core having about an 1811 size of 3c8 material and includes a third winding coupled to said power circuit, said first winding having about 132 turns of about 37 gauge wire, said second winding having about 308 turns of about 34 gauge wire and said third winding having about 315 turns of about 36 gauge wire.

18. The monitor and control interface of claim 12 wherein said isolation transformer includes a core and means, coupled to said core, for producing about 2 to 12 watts from an input digital signal having about 40 to about 100 volts peak-to-peak operated at an average frequency range of about 500 hertz to about 20,000 hertz.

19. The monitor and control interface of claim 12 wherein said adapter-network interface includes a current transmitter and said power circuit includes a twenty four volt regulator for operation of said current transmitter.

20. The monitor and control interface of claim 12 wherein said sensor-controller interface includes means for converting current signals received from said at least one network device to voltage levels for transmission to a network controller.

21. The monitor and control interface of claim 12 wherein said adapter-network interface includes a non-volatile RAM for storing configuration data.

22. The monitor and control interface of claim 12 further comprising an ambient temperature sensor for providing an ambient temperature signal wherein said adapter-network interface includes means, responsive to said ambient temperature signal, for compensating for temperature drift.

23. The monitor and control interface of claim 22 wherein said ambient temperature signal is provided to said adapter-network interface for transmission to a controller.

24. The monitor and control interface of claim 12 wherein said power circuit includes at least one device to accumulate charge to operate the monitor and control interface between receipt of power-data packets at said second winding.

25. The monitor and control interface of claim 12 further comprising means, coupled to said power circuit, said adapter-network controller and said sensor-controller interface for conserving power by entering low-power mode upon occurrence of a predetermined event.

26. The monitor and control interface of claim 12 further comprising a current transmitter and means, coupled to said current transmitter and to said sensor-controller interface, for operating both said current transmitter and said at least one network device concurrently.

27. The monitor and control interface of claim 13 further comprising means, coupled to said transmitting means, for dc-balancing said transmitted information.

28. A network, comprising:

at least one network controller, said at least one network controller comprising:

a power circuit;

a communications circuit, coupled to said power circuit, for transmitting a power-data packet and for receiving data relative to a port of said network controller; and

a user-network interface controller, coupled to said power circuit and to said communication circuit, for processing data for transmission by said communication circuit by implementing a dc-balancing mechanism to substantially dc-balance transmissions of said communication

circuit;

at least one network device;

at least one monitor and control interface coupled to said at least one network device, said at least one monitor and control interface comprising:

an isolation transformer;

a power circuit, coupled to a first winding of said isolation transformer, for receipt of a transformer-coupled power-data packet transmitted to a second winding of said isolation transformer to generate operating power from said transformer-coupled power-data packet for the monitor and control interface;

a sensor-controller interface, powered by said power circuit, for interfacing said at least one network device which includes providing power to operate said at least one network device; and

an adapter-network interface coupled to said first winding and to said sensor-controller interface, said adapter-network interface powered by said power circuit and responsive to said transformer-coupled power-data packet to control operation of the monitor and control interface; and

a first conductive medium coupling said port of said network controller to said isolation transformer of each said monitor and control interface to provide power-data from said network controller to each said at least one monitor and control interface.

29. The network of claim 28 wherein said first conductive medium provides data from each said monitor and control apparatus to said network controller.

30. The network of claim 28 wherein said data for transmission includes at least one byte and wherein said dc-balancing mechanism includes a look-up table responsive to said at least one byte, said look-up table storing a particular predefined balancing character for said at least one byte which substantially dc-balances said at least one byte, said dc-

balancing mechanism appending said predefined balancing character to said at least one byte for transmission.

31. The network of claim 28 wherein said data for transmission includes at least one byte including a plurality of bits and wherein said dc-balancing mechanism includes means for producing an inverted byte wherein said inverted byte has a plurality of bits with each bit of said inverted byte equivalent to an inversion of each bit of said plurality of bits of said at least one byte, said dc-balancing mechanism providing said inverted byte to said communication circuit so said communication circuit can transmit said at least one byte and said inverted byte.

32. The network of claim 30 further comprising a power-data balance monitor coupled to a winding of said isolation transformer and to said user-network interface controller, for detecting a net dc-imbalance at said isolation transformer winding and asserting a signal to said user-network interface controller when it detects a dc-imbalance to influence said dc-balancing mechanism.

33. The network of claim 30 wherein said network controller further comprises a power-data balance monitor coupled to a winding of said isolation transformer and to said user-network interface controller, for detecting a net dc-imbalance at said isolation transformer winding and asserting a signal to said user-network interface controller when it detects a dc-imbalance to alter said predefined balancing byte appended to said at least one byte.

34. The network of claim 28 wherein said transmitted power-data packet includes an address field and a command field and wherein said at least one monitor and control interface has a particular address and each said at least one monitor and control interface is responsive to command data in said command field of said transmitted power-data packet if address data in said address field corresponds to said particular address.

35. The network of claim 34 wherein said command data causes said monitor and control interface to operate said at least one network device.

36. The network of claim 35 wherein said network device is a sensor and said operation of said network device measures an environmental parameter of said sensor.

37. The network of claim 35 wherein said network device is an actuator and said operation of said network device initiates an action of said network device.

38. The network of claim 35 wherein said power circuit of said monitor and control interface includes at least one device for accumulating charge extracted from said transmitted power-data packet.

39. The network of claim 38 wherein said monitor and control interface transmits data to said network controller in response to said command data wherein said stored charge is sufficient for said transmission to said network.

40. The network of claim 38 wherein said monitor and control interface initiates data transmission to said network controller responsive to some predetermined condition of said at least one network device.

41. The network of claim 34 wherein each power circuit of each said at least one monitor and control interface includes a storage device for accumulating charge for operation of each said monitor and control interface and said network controller periodically transmits power-data packets to said at least one monitor and control interface to maintain a level of stored charge in each said storage device sufficient to operate, including responding to said command data, said monitor and control interface until a next transmission of a power-data packet to said monitor and control interface.

42. The network of claim 35 wherein said at least one monitor and control interface initiates a condition transmission in response to a predetermined condition without receipt of a power-data packet commanding a particular activity.

43. The network of claim 42 wherein said network controller is responsive said condition transmission to transmit a power-data packet to said at least one monitor and control interface to recharge said storage device of said transmitting at least one monitor and control interface.

44. The network of claim 28 further comprising at least a second network controller coupled to said at least one monitor and control interface by said first conductive medium.

45. The network of claim 44 wherein said first network controller is coupled to a first end of said conductive medium and said second network controller is coupled to a second end of said conductive medium.

46. The network of claim 44 further comprising at least a second monitor and control interface wherein said first conductive medium couples said at least one network controller to said first and said second monitor and control interface in a first order and wherein said first conductive medium couples said at least a second network controller to said first and said second monitor and control interface in a second order such that said at least one network controller and said at least a second network controller can interface with both said at least one monitor and control interface and said at least a second monitor and control interface if said first conductive medium has a fault between said monitor and control interfaces.

47. The network of claim 28 further comprising a second conductive medium coupling said port of said at least one network controller to said at least one monitor and control interface.

48. A network, comprising:

at least one network controller, said at least one network controller comprising:

a power circuit;

a communications circuit, coupled to said power circuit, for transmitting a power-data packet and for receiving data relative to a port of said network controller; and

a user-network interface controller, coupled to said power circuit and to said communication circuit, for processing data for transmission by said communication circuit by implementing a dc-balancing mechanism to substantially dc-balance transmissions of said communication circuit;

at least two network devices;

at least two monitor and control interfaces, with a first one network device coupled to a first one monitor and control interface and a second one network device coupled to a second one monitor and control interface, each said at least two monitor and control interfaces comprising:

an isolation transformer;

a power circuit, coupled to a first winding of said isolation transformer, for receipt of a transformer-coupled power-data packet transmitted to a second winding of said isolation transformer to generate operating power from said transformer-coupled power-data packet for the monitor and control interface;

a sensor-controller interface, powered by said power circuit, for interfacing said at least one network device which includes providing power to operate said at least one network device; and

an adapter-network interface coupled to said first winding and to said sensor-controller interface, said adapter-network interface powered by said power circuit and responsive to said transformer-coupled power-data packet to control operation of the monitor and control interface; and

a first conductive medium coupling said port of said network controller to said isolation transformer of each said monitor and control interface to provide power-data from said network controller to each said at least one monitor and control interface.

49. The network of claim 48 wherein said transmitted power-data packet includes an address field and a command field and wherein each said at least two monitor and control interfaces has a first particular address and each said at least two monitor and control interfaces is responsive to command data in said command field of said transmitted power-data packet if address data in said address field corresponds to said first particular address.

50. The network of claim 49 wherein said first particular address of said first monitor and control interface is unique relative to said first particular address of said second monitor and control interface such that said network controller can independently operate each of said at least two monitor and control interfaces.

51. The network of claim 49 wherein each said at least two monitor and control interfaces includes a second particular address.

52. The network of claim 51 wherein said second particular address of said second monitor and control interface corresponds to said first particular address of said first monitor and control interface.

53. The network of claim 52 wherein said second monitor and control interface is responsive to status information transmitted from said first monitor and control interface to operate said second network device.

54. A network, comprising:

a monitor;

a power source;

a network device;

a network controller, coupled to said monitor and to said power source, said network controller including a first isolation transformer and a power-data balance circuit coupled to a port, said network controller responsive to a signal from said power-data balance circuit to output dc-balanced data at said port; and

a network device adapter, coupled to said network device, said network device adapter including a second isolation transformer coupled to said port of said network controller for receiving balanced data having amplitude and pulse width characteristics sufficient to power said network device adapter and said network device.

55. The network of claim 54 wherein said first and second isolation transformers are substantially functionally equivalent.

56. The network of claim 55 wherein said first and second isolation transformers are substantially identical.

57. A network, comprising:

a monitor;

a power source;

a network device;

a network controller, coupled to said monitor and to said power source, said network controller including:

a first isolation transformer having a first winding a second winding and a third winding, with said second winding coupled to a port of said network controller;

a power source;

a communication circuit, coupled to said isolation transformer and to said power source, for transceiving data, said communication circuit including a power-data transmitter part coupled to said port and responsive to a first control signal, for producing and transmitting power-data having a particular amplitude and pulse-

width characteristic, said communication circuit including a receiver part coupled to said first winding for receipt of data input to said port;

a power-data balance monitor, coupled to said third winding, for sensing a net dc-imbalance per particular sample time of a packet of transmitted output power-data, said balance monitor asserting a net high signal when said transmitted packet has a positive net dc-balance and said balance monitor asserting a net low signal when said transmitted packet has a negative net dc-balance; and

a user-network interface controller, coupled to said power source, said power-data balance monitor and to said communication circuit, for controlling operation of said network controller, said interface controller responsive to an assertion of said net high signal to command said communication circuit to transmit additional negative dc pulses appended to said packet until a net dc-balance of transmitted power-data is substantially zero, said user-network interface responsive to an assertion of said net low signal to command said communication circuit to transmit positive dc pulses appended to said transmitted packet until said net dc-balance of transmitted power-data is substantially zero; and

a network device adapter, coupled to said network device, said network device adapter including a second isolation transformer coupled to said port of said network controller for receiving said net dc-balanced power-data with said particular amplitude and pulse width characteristic sufficient to power said network device adapter and said network device.

58. A network controller for a network including a plurality of network devices for sensing and effecting environmental parameters, with each of the plurality of network devices powered, addressed and accessed over a common conductive medium through one of a plurality of adapter units, the network controller comprising:

an isolation transformer having a first and second winding, with the second winding coupled to the conductive medium at a port;

a power supply including a current monitor for asserting an excess current signal when a prespecified current level is exceeded;

a communication circuit coupled to said isolation transformer and to said power supply and responsive to a transmit signal and a data signal having at least one byte, said communication circuit comprising:

a data receiver, coupled to said first winding of said isolation transformer, for receiving a response signal from a particular one of the plurality of network devices connected to an addressed one of the plurality of adapter units;

a data transmitter, coupled to said port, for asserting and deasserting digital power-data signals according to said data signal if said transmit signal is asserted and said excess current signal is deasserted; and

a snubber circuit, coupled to said port, for damping ringing manifested at said port for a prespecified time interval upon a deassertion of said transmit signal;

a user-network interface coupled to said power supply and said communication circuit comprising:

a user interface for receiving an instruction from a monitor and for transmitting a network status signal to said monitor; and

a network interface for asserting and deasserting said data signal and said transmit signal responsive to a predetermined program and to said instruction, said network interface including means for appending a balancing byte having a number of bits to each said byte of said data signal to substantially reduce a dc-imbalance in each of a plurality of isolation transformers coupling each of the plurality of adapter units to the conductive medium, said appending means responsive to a balancing signal to adjust said number of bits of said balancing byte appended to each byte of said data signal; and

a digital power-data balancing monitor, coupled to a third winding of said isolation transformer and to said network interface, for detecting an actual net dc-imbalance and for asserting said balance signal to said network interface if said actual net dc-imbalance is detected.

59. A snubber circuit for dissipating charge stored in an isolation transformer as a result of transmission of power-data, comprising:

a switch;

an impedance in series with said switch with said series coupled switch and impedance coupled across a winding of the isolation transformer; and

a switch control circuit, responsive to a signal terminating transmission of power-data, for selectively engaging said switch for a predetermined time interval after assertion of said signal.

60. A method for operating a network having a network controller that includes a communication circuit, a power circuit and a user-network interface controller and a first monitor and control interface for interfacing a first network device, comprising the steps of:

transmitting dc-balanced power-data to the first monitor and control interface which includes an isolation transformer;

extracting power and command data imbedded in said transmitted power-data; and

operating said network device, including powering and control functions, from said transmitted power-data.

61. A method for transmitting a data packet, including a data byte having a plurality of bits, from a network controller having a power circuit and a communications circuit, comprising the steps of:

accessing the data byte to be transmitted;

reading a balancing byte corresponding to the data byte from a look-up table;

appending said balancing byte to the data packet; and

operating a driver circuit coupled to a port of the network controller with the data byte and said appended balancing byte at a sufficient amplitude to operate monitor and control interface coupled to said port.

62. A method for forming a data packet, including a data byte having a plurality of bits, from a network controller having a power circuit and a communications circuit, comprising the steps of:

processing the data byte to establish a net imbalance in bit sense of the data packet; and

appending a balancing byte to the data byte to reduce said net bit sense imbalance.

63. The method of claim 62 further comprising the step of operating a driver circuit coupled to a port of the network

controller with the data byte and said appended balancing byte at a sufficient amplitude to operate monitor and control interface coupled to said port.

5

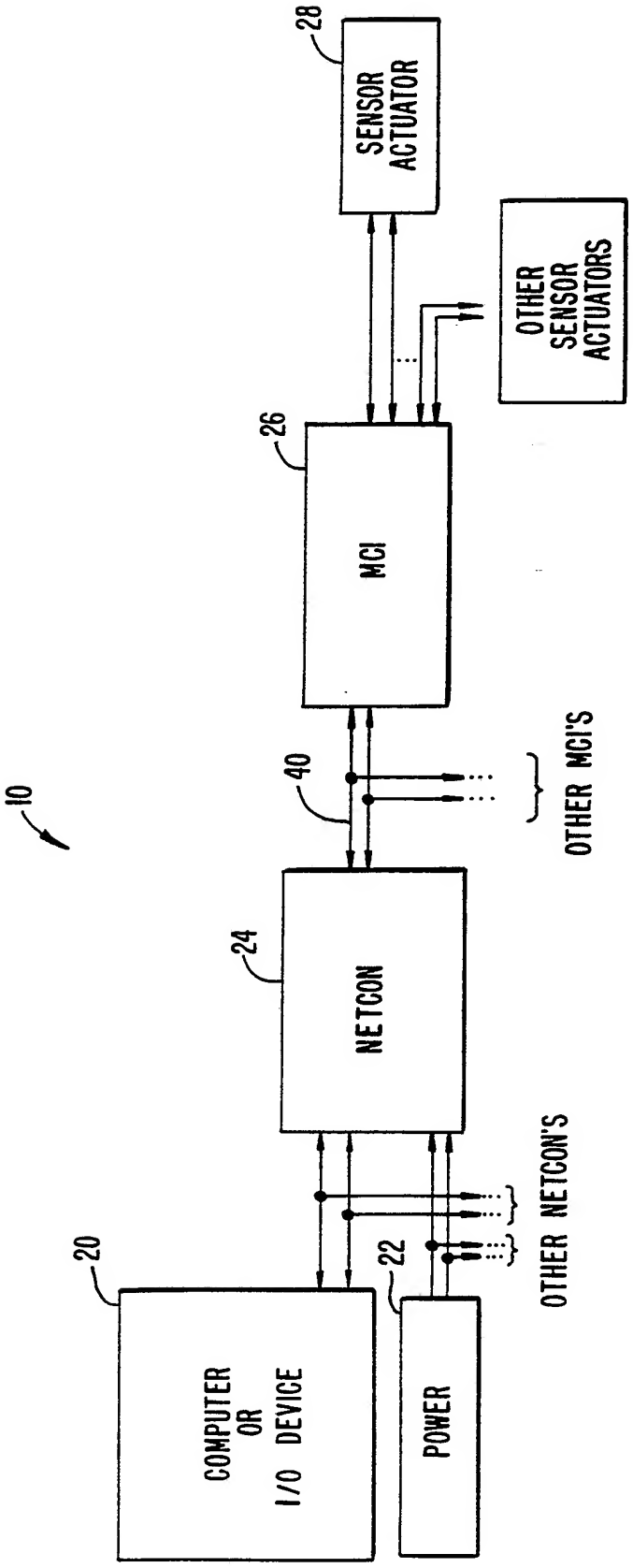
10
20
COMPUTER OR I/O DEVICE
22
POWER
24
NETCON
OTHER NETCON'S
26
MCI
OTHER MCI'S
28
SENSOR ACTUATOR
OTHER SENSOR ACTUATORS
40

FIG. 1.

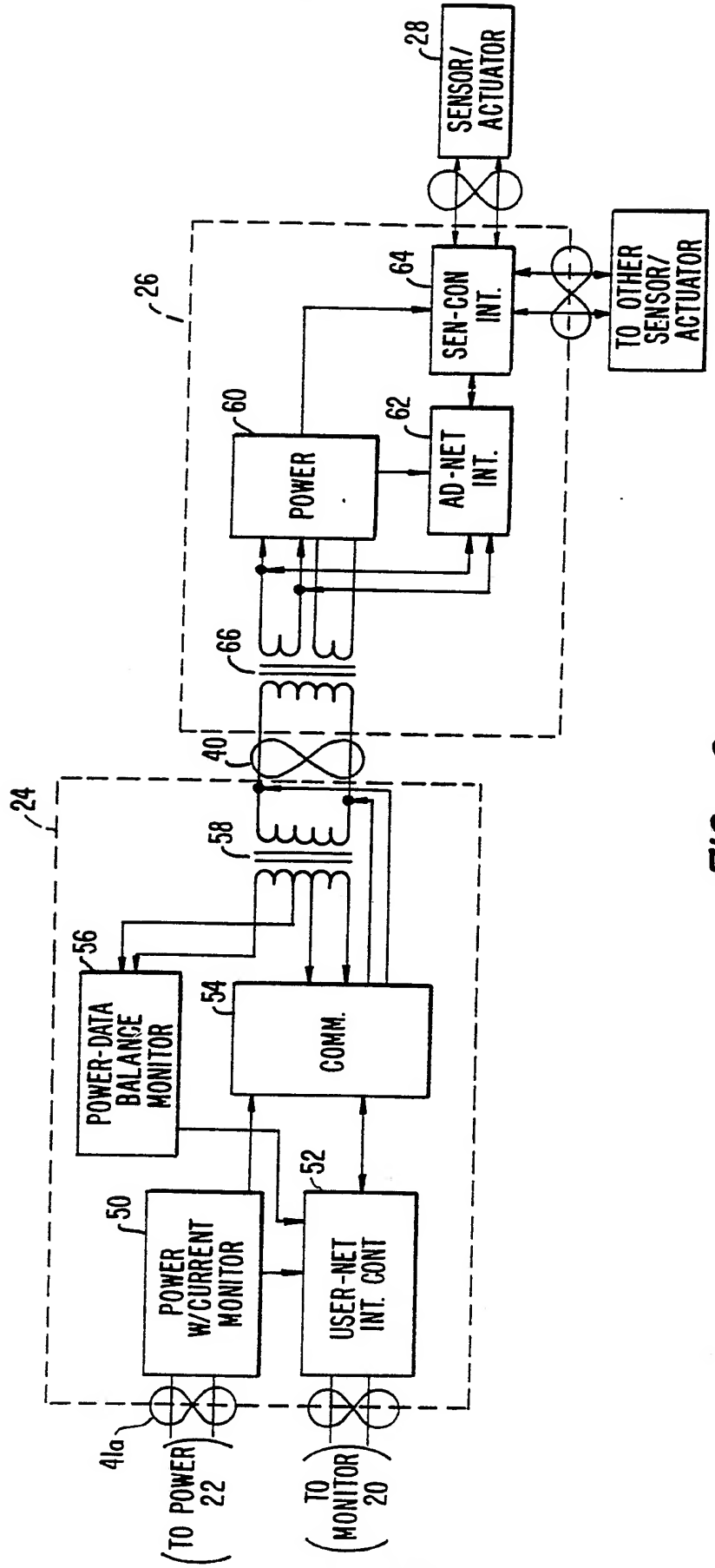
28
SENSOR/ ACTUATOR
26
64
SEN-CON INT.
TO OTHER SENSOR/ ACTUATOR
60
POWER
62
AD-NET INT.
66
40
24
58
56
POWER-DATA BALANCE MONITOR
54
COMM.
52
50
POWER W/CURRENT MONITOR
USER-NET INT. CONT
41a
(TO POWER 22)
(TO MONITOR 20)

FIG. 2.

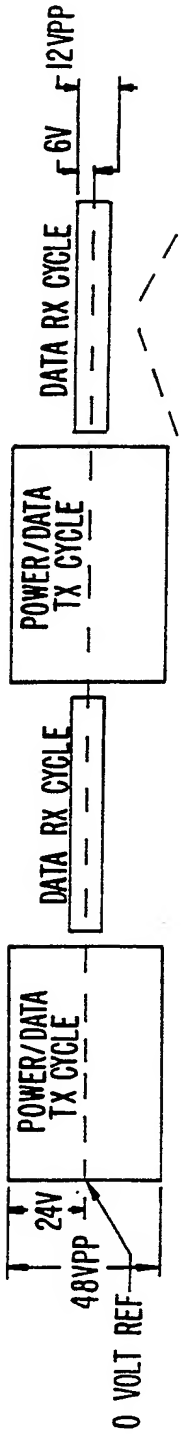

FIG. 3.

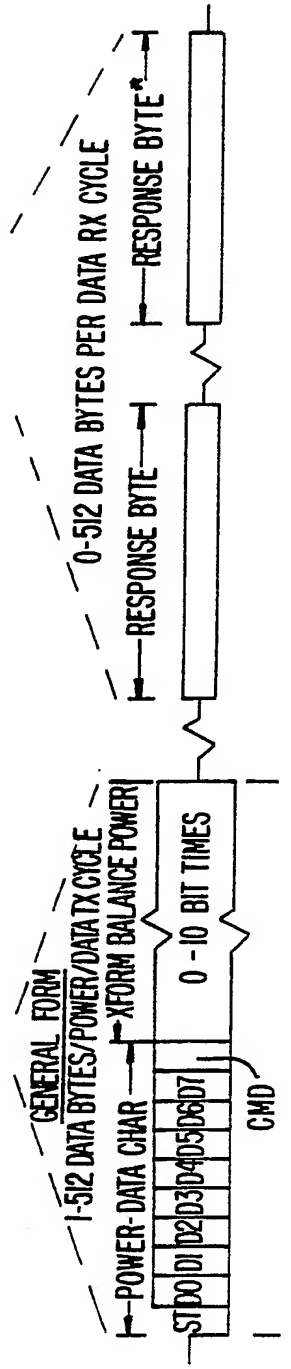

FIG. 4.

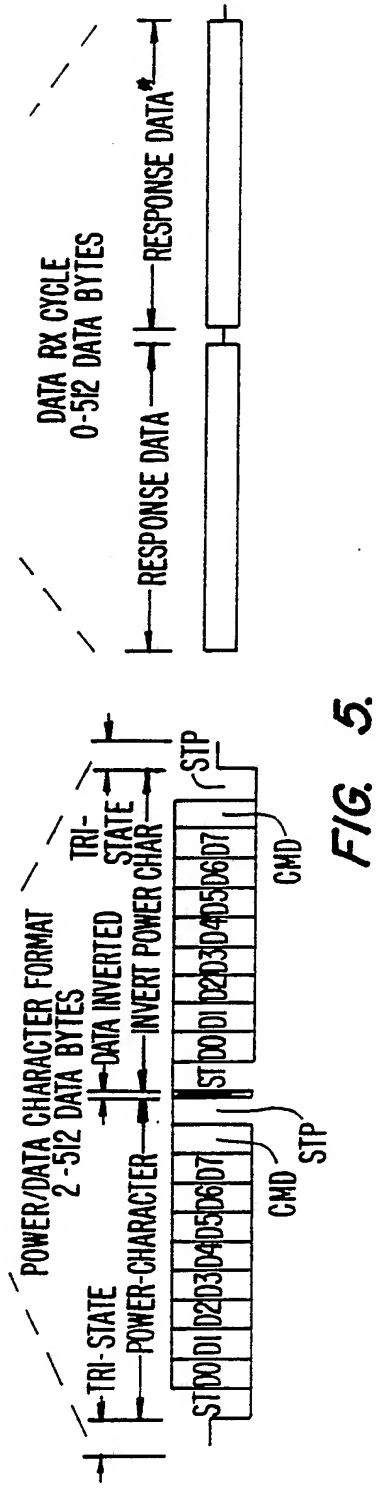

FIG. 5.

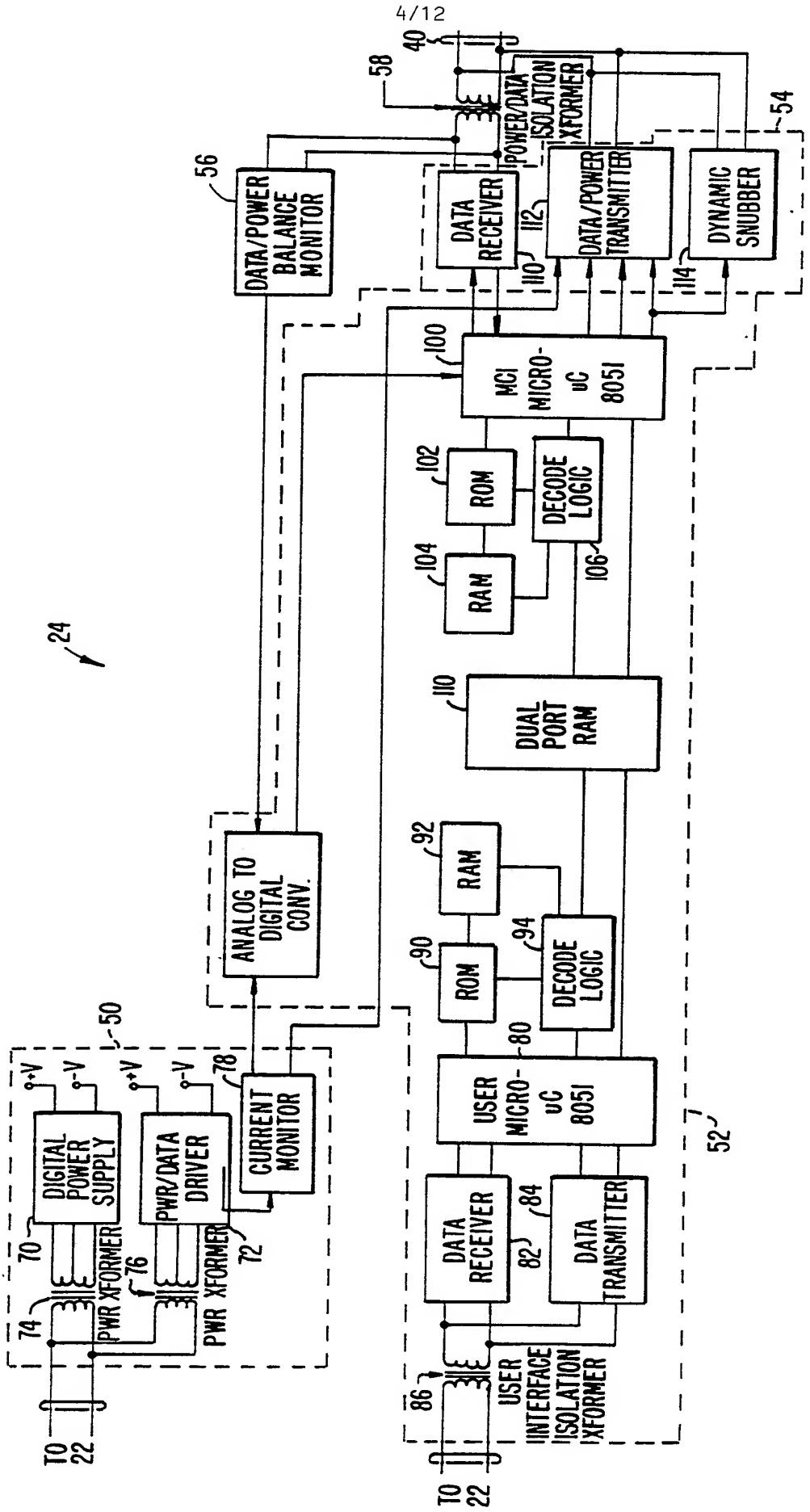
24
40
58
POWER/DATA ISOLATION XFORMER
54
56
DATA/POWER BALANCE MONITOR
DATA RECEIVER
112
DATA/POWER TRANSMITTER
DYNAMIC SNUBBER
110
114
100
MCI MICRO- uC 8051
102
ROM
DECODE LOGIC
104
RAM
106
110
DUAL PORT RAM
ANALOG TO DIGITAL CONV.
92
RAM
90
ROM
94
DECODE LOGIC
80
USER MICRO- uC 8051
52
50
+V
-V
+V
-V
78
DIGITAL POWER SUPPLY
PWR/DATA DRIVER
CURRENT MONITOR
70
72
74
76
PWR XFORMER
PWR XFORMER
TO 22
DATA RECEIVER
82
84
DATA TRANSMITTER
86
USER INTERFACE ISOLATION XFORMER
TO 22

FIG. 6.

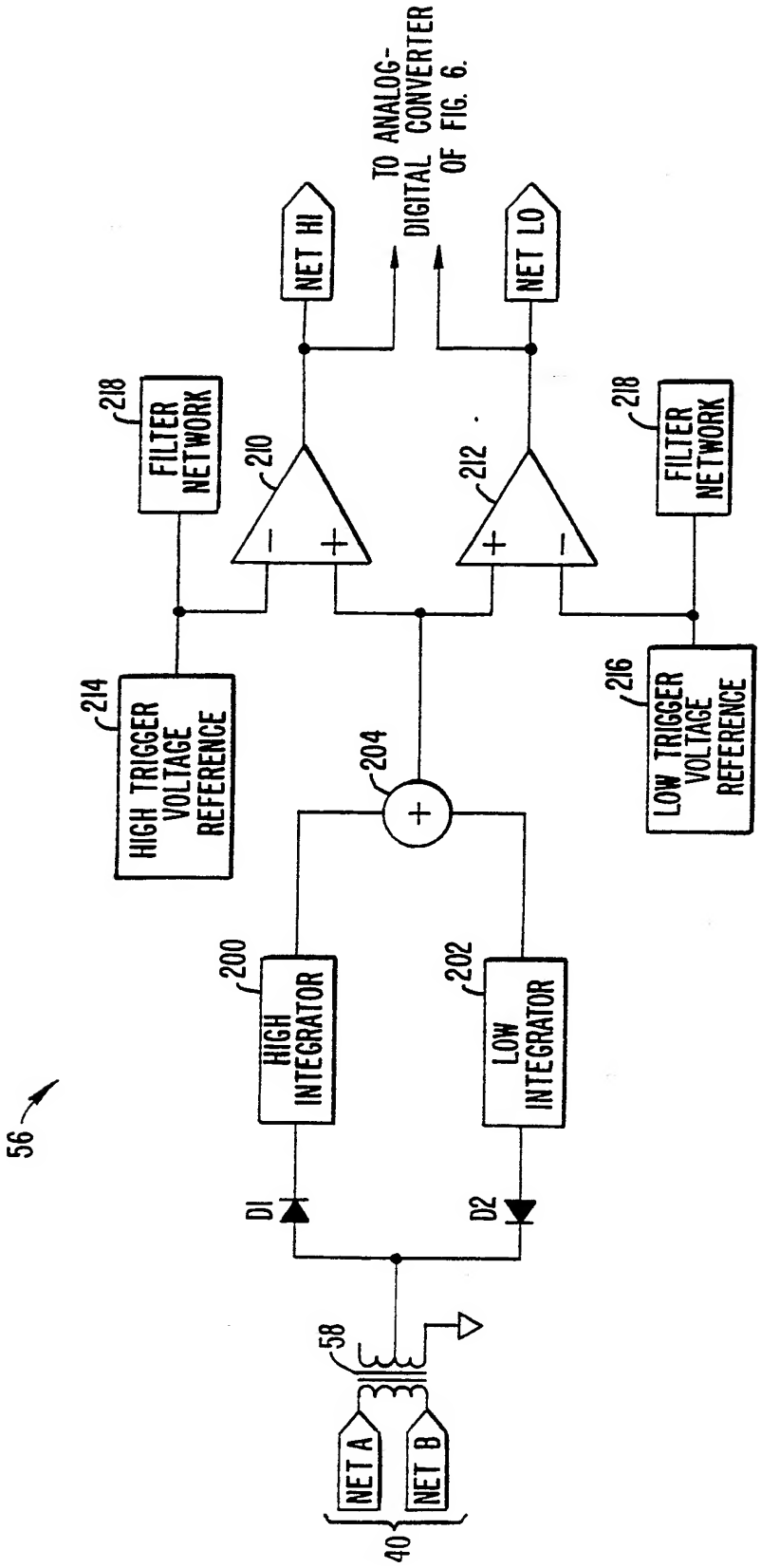
TO ANALOG-DIGITAL CONVERTER OF FIG. 6.
NET HI
NET LO
218
FILTER NETWORK
218
FILTER NETWORK
210
212
214
HIGH TRIGGER VOLTAGE REFERENCE
216
LOW TRIGGER VOLTAGE REFERENCE
204
200
HIGH INTEGRATOR
202
LOW INTEGRATOR
56
D1
D2
58
NET A
NET B
40

FIG. 7.

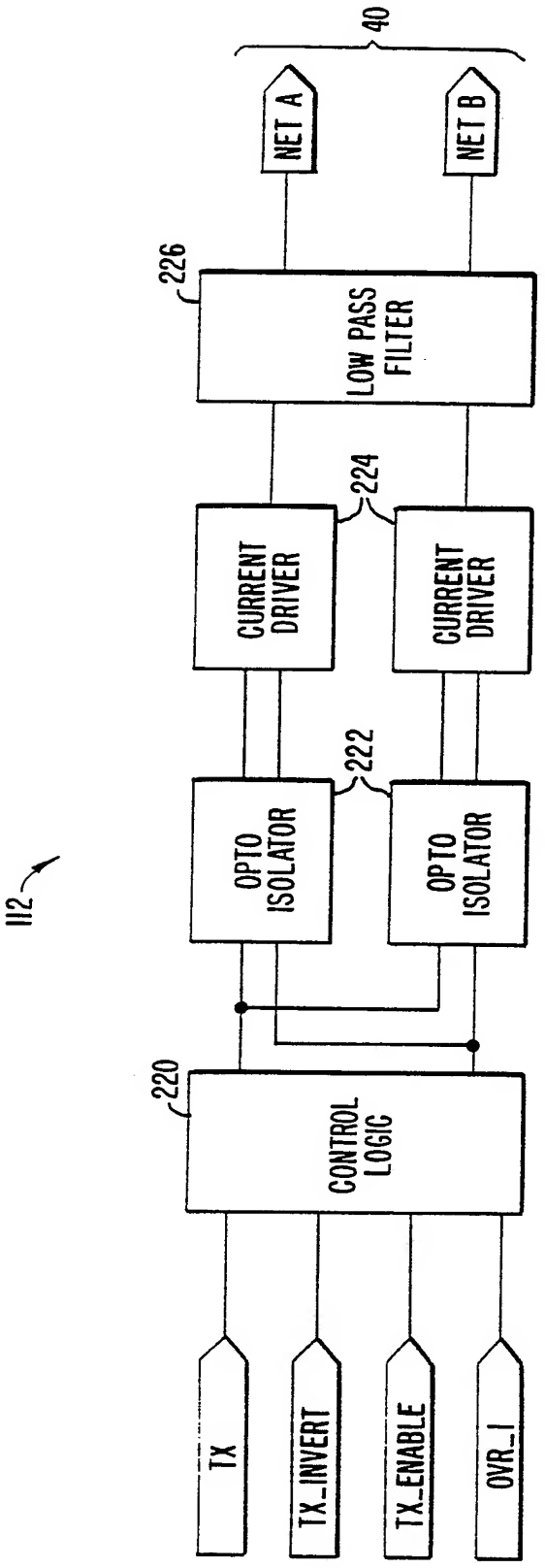
40
NET A
NET B
226
LOW PASS FILTER
224
CURRENT DRIVER
CURRENT DRIVER
222
OPTO ISOLATOR
OPTO ISOLATOR
112
220
CONTROL LOGIC
TX
TX_INVERT
TX_ENABLE
OVR_I

FIG. 8.

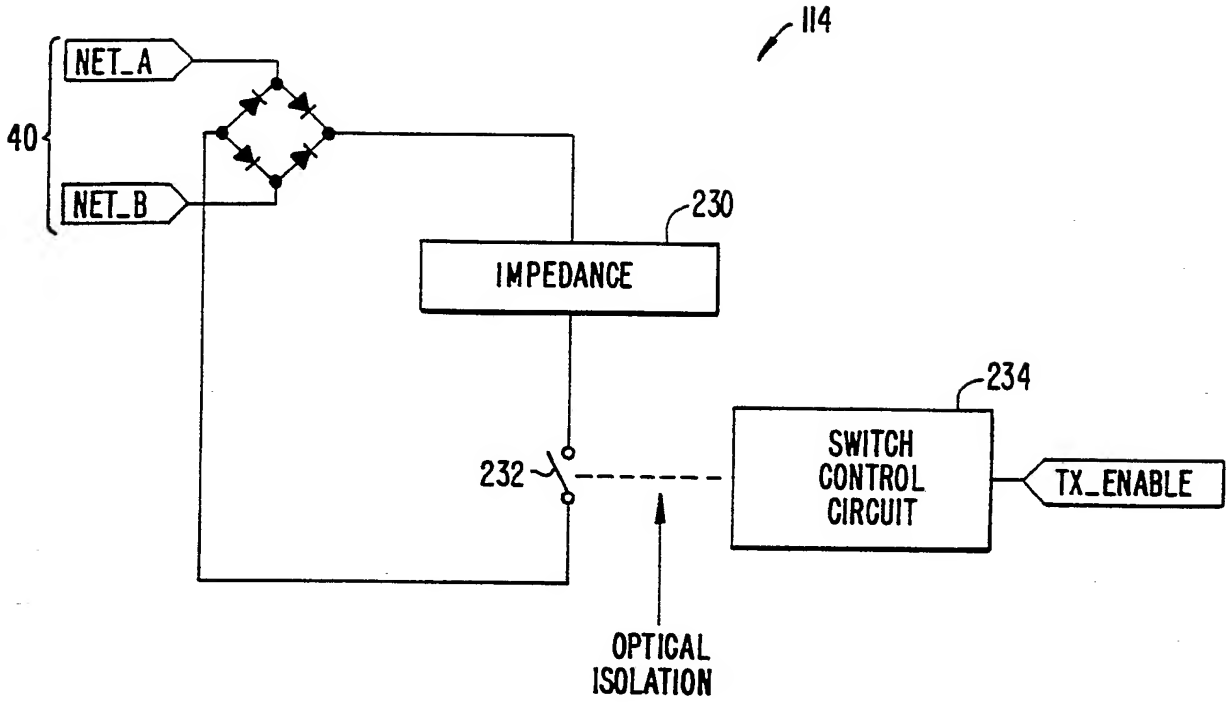
114
NET_A
40
NET_B
230
IMPEDANCE
234
SWITCH
CONTROL
CIRCUIT
TX_ENABLE
232
OPTICAL
ISOLATION

FIG. 9A.

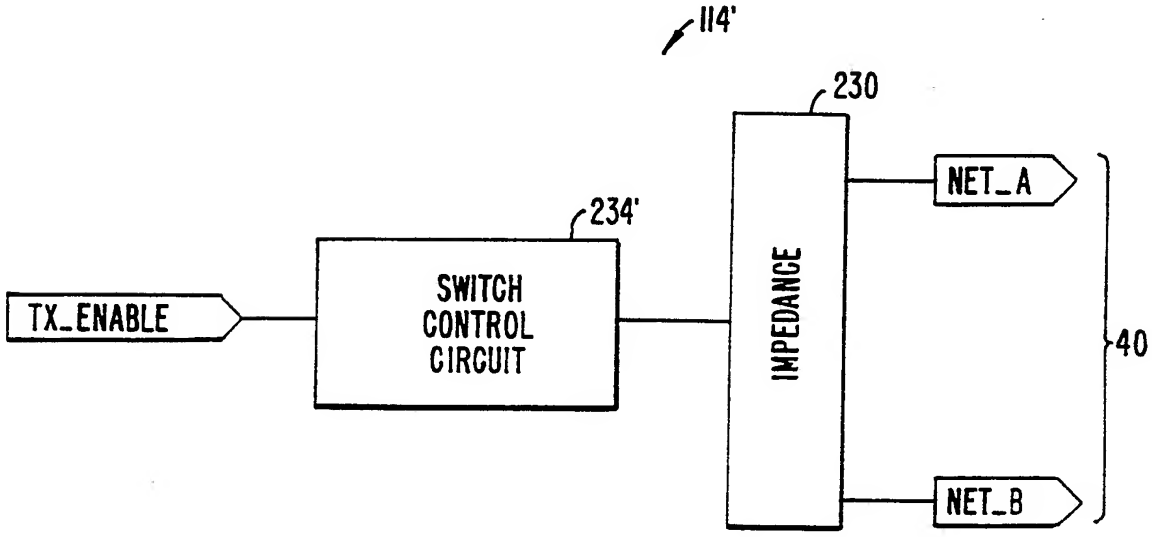
114'
230
NET_A
234'
SWITCH
CONTROL
CIRCUIT
IMPEDANCE
TX_ENABLE
40
NET_B

FIG. 9B.

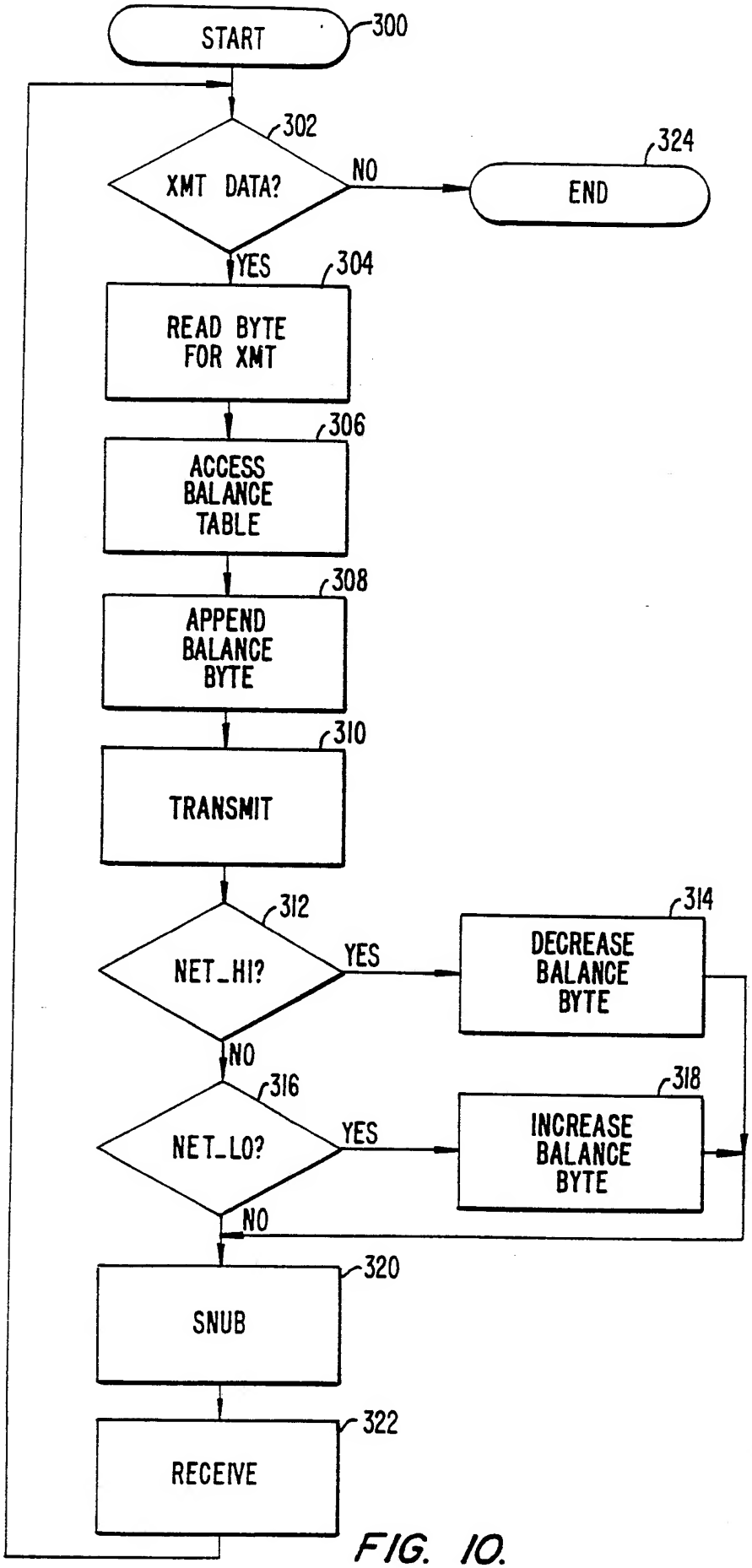
START
300
302
XMT DATA?
NO
324
END
YES
304
READ BYTE FOR XMT
306
ACCESS BALANCE TABLE
308
APPEND BALANCE BYTE
310
TRANSMIT
312
NET_HI?
YES
314
DECREASE BALANCE BYTE
NO
316
NET_LO?
YES
318
INCREASE BALANCE BYTE
NO
320
SNUB
322
RECEIVE

FIG. 10.

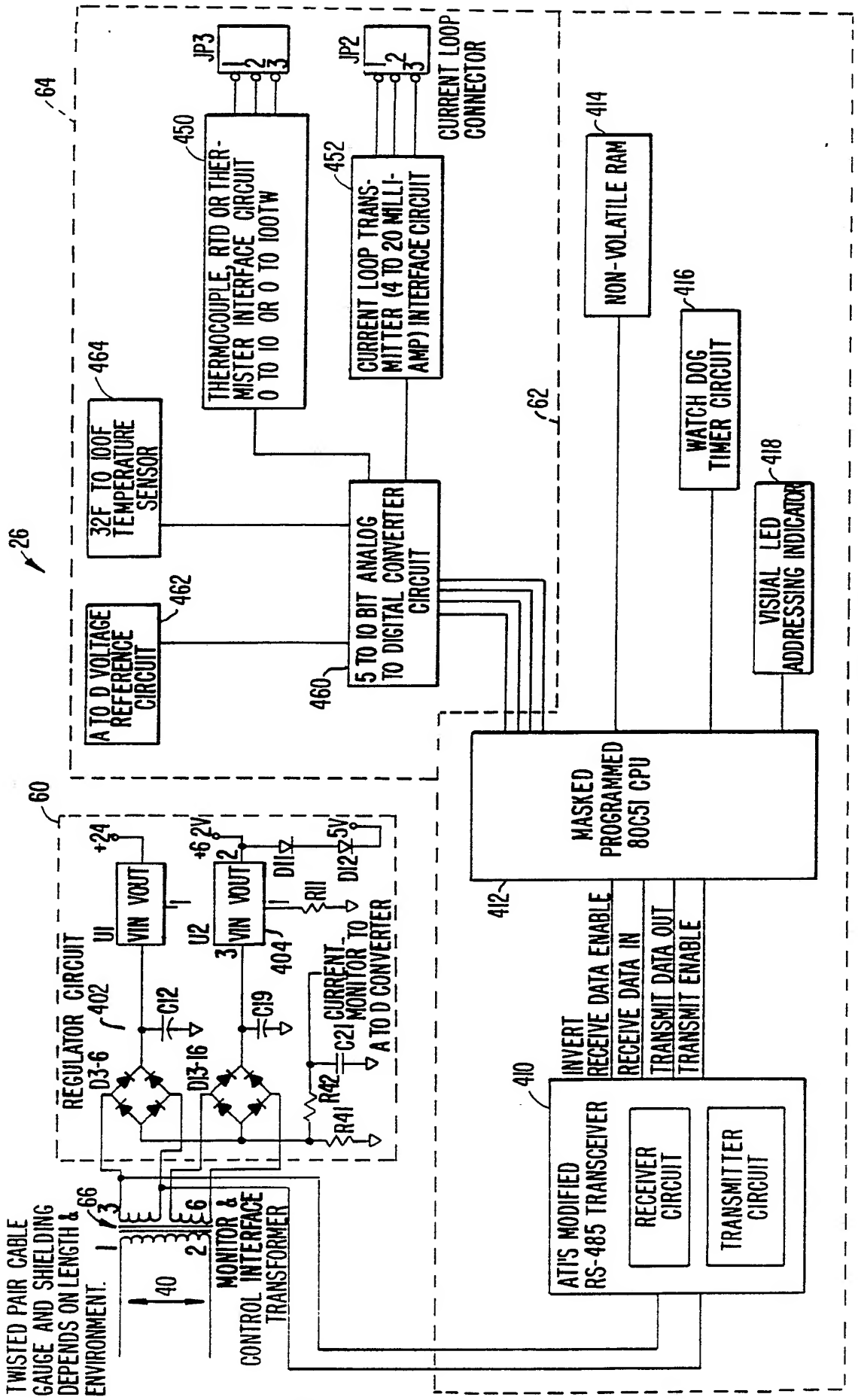
64
JP3
JP2
CURRENT LOOP CONNECTOR
450
THERMOCOUPLE, RTD OR THERMISTER INTERFACE CIRCUIT 0 TO 10 OR 0 TO 100TW
452
CURRENT LOOP TRANSMITTER (4 TO 20 MILLIAMP) INTERFACE CIRCUIT
414
NON-VOLATILE RAM
416
WATCH DOG TIMER CIRCUIT
418
VISUAL LED ADDRESSING INDICATOR
464
32F TO 100F TEMPERATURE SENSOR
462
A TO D VOLTAGE REFERENCE CIRCUIT
460
5 TO 10 BIT ANALOG TO DIGITAL CONVERTER CIRCUIT
26
62
60
+24
+6.2V
5V
U1
VIN VOUT
U2
VIN VOUT
D11
D12
R11
REGULATOR CIRCUIT
402
C12
C19
404
CURRENT MONITOR TO A TO D CONVERTER
C21
D3-6
D3-16
R42
R41
412
MASKED PROGRAMMED 80C51 CPU
410
INVERT
RECEIVE DATA ENABLE
RECEIVE DATA IN
TRANSMIT DATA OUT
TRANSMIT ENABLE
ATIS MODIFIED RS-485 TRANSCEIVER
RECEIVER CIRCUIT
TRANSMITTER CIRCUIT
66
MONITOR & CONTROL INTERFACE TRANSFORMER
40
TWISTED PAIR CABLE GAUGE AND SHIELDING DEPENDS ON LENGTH & ENVIRONMENT.

FIG. 11.

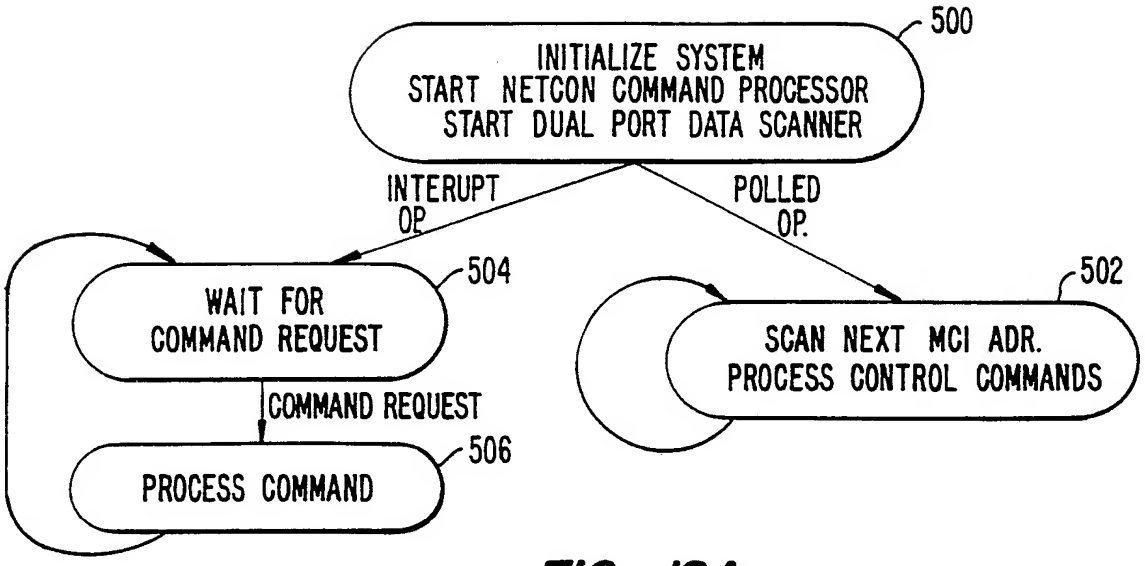

FIG. 12A.

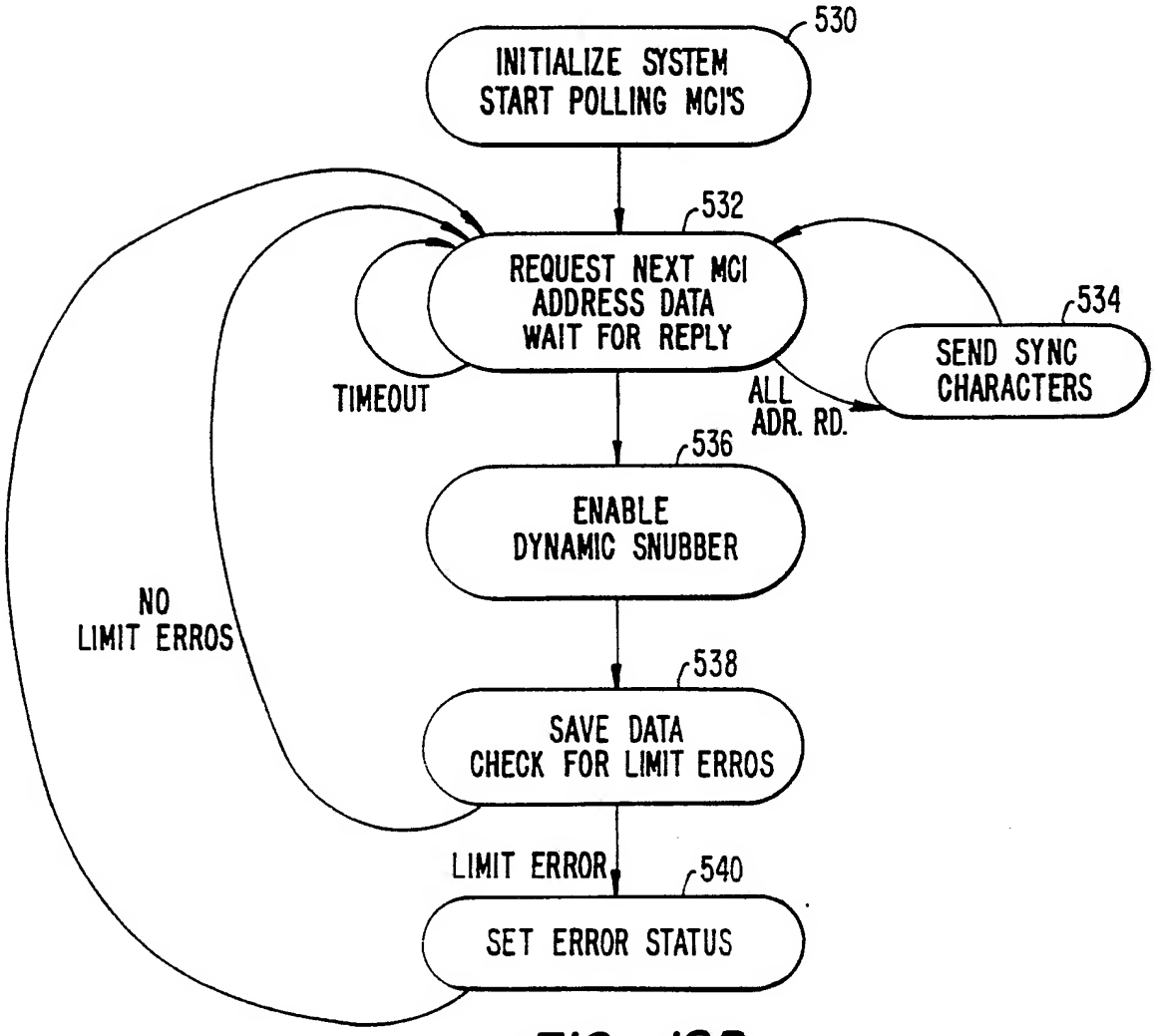

FIG. 12B.

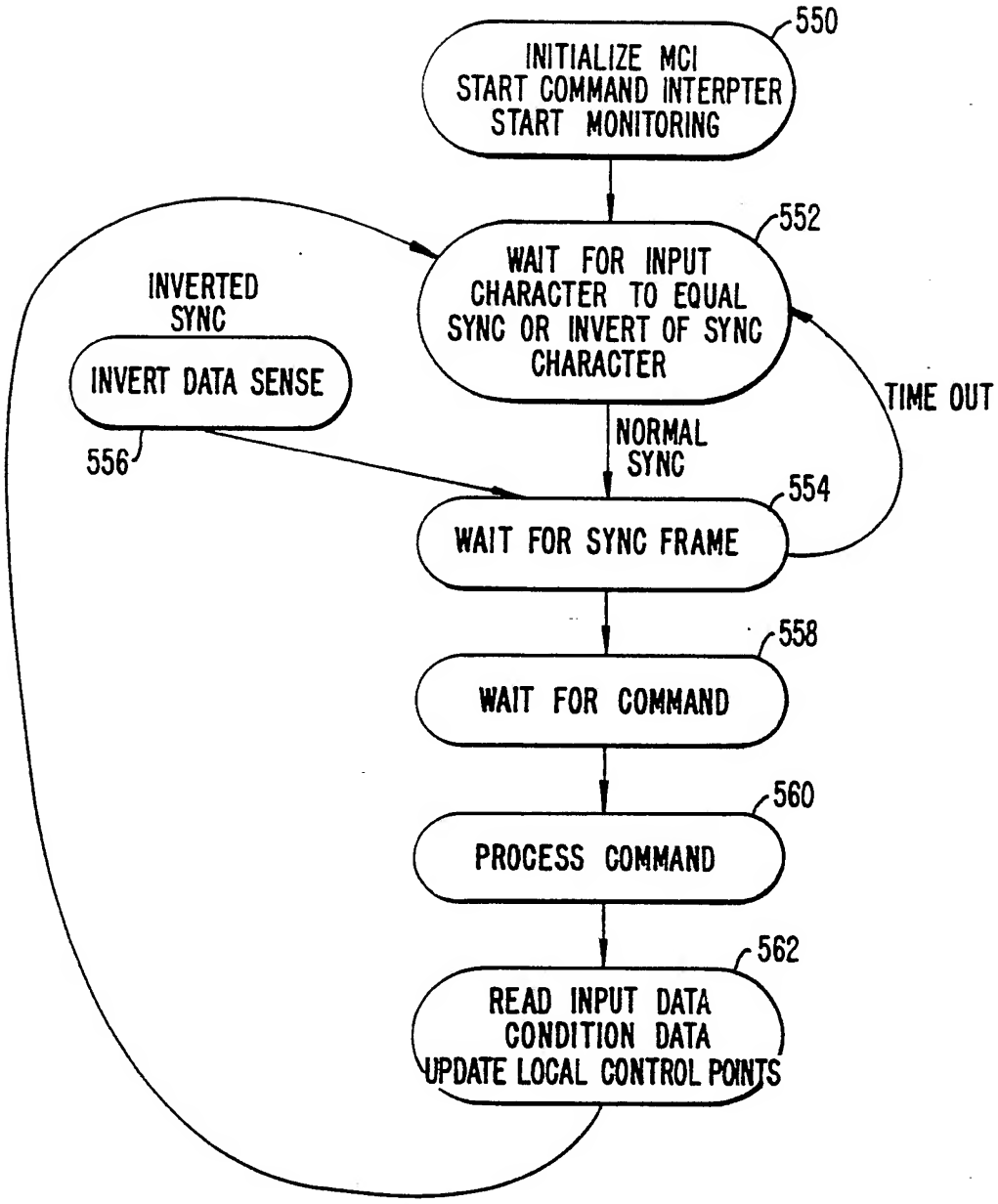
550
INITIALIZE MCI
START COMMAND INTERPTER
START MONITORING
552
WAIT FOR INPUT
CHARACTER TO EQUAL
SYNC OR INVERT OF SYNC
CHARACTER
INVERTED
SYNC
INVERT DATA SENSE
556
TIME OUT
NORMAL
SYNC
554
WAIT FOR SYNC FRAME
558
WAIT FOR COMMAND
560
PROCESS COMMAND
562
READ INPUT DATA
CONDITION DATA
UPDATE LOCAL CONTROL POINTS

FIG. 12C.

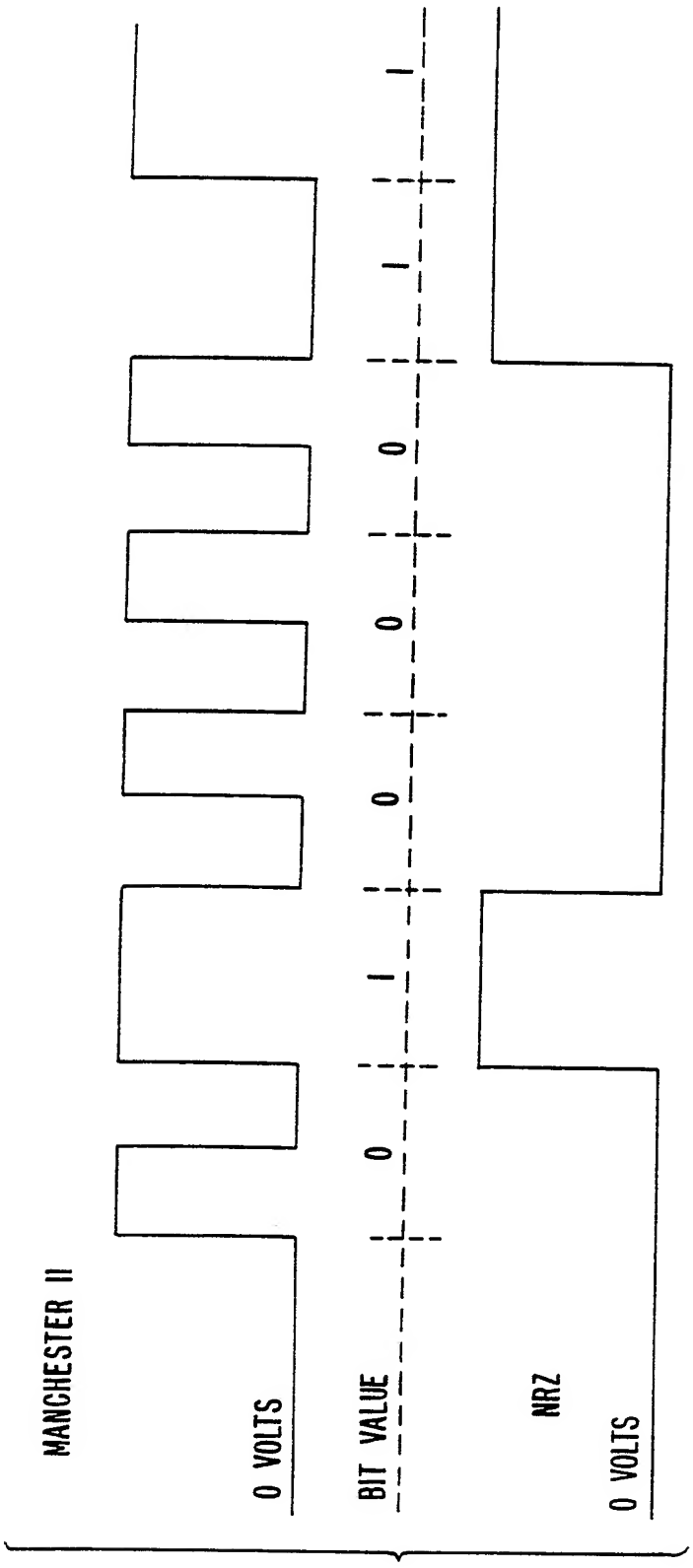

FIG. 13.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05926

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04L 27/00
US CL :375/37,7; 340/825.07 340/310A, 310R
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/76,19, 340/825.06, 825.17 340/825.55, 310A, 310R, 500, 505; 370/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,973,954 (SCHWARZ) 27 NOVEMBER 1990 See figures 1a,1b and 2.	1-61
A,P	US,A, 5,084,868 (KELLY ET AL) 28 JANUARY 1992 See figure 1.	1,12,28,48,54 57-61

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 16 SEPTEMBER 1992	Date of mailing of the international search report 16 NOV 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer T. BOCURE Telephone No. (703) 305-5926

Form PCT/ISA/210 (second sheet)(July 1992)★

B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

USPTO APS Isolat ### Transformer, Network Controller, Sensor, Actuators or Actuator, Monitor, Control, Powering or Power Source or Power Circuit, DC Balance ###, Snubber Circuit, Switch, Switch ### Control, Power Data